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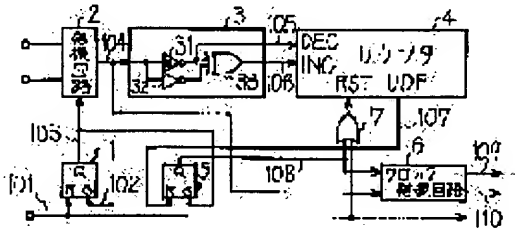
(54) STANDBY CONTROL CIRCUIT

(57)Abstract:
PURPOSE: To secure a startup stable time at the time of resonator operation, and to eliminate an unnecessary oscillation time at the time of external clock supply operation and improve response by controlling the operation of a clock generating circuit with the signal outputted from a flip-flop.
CONSTITUTION: The signal 103 outputted from the flip-flop 1 and the underflow signal 107 outputted from a counter 4 are inputted and a signal 108 is outputted and inputted to the clock generating circuit 6 and an OR gate 7. The operation of the clock generating circuit 6 is controlled with the signal 108 and the resetting of a counter 4 is controlled. The clock generating circuit 6 inputs the clock signal 104 outputted from an oscillation circuit 2 and outputs specific clock signals 109 and 110 on the basis of the clock signal 104. Consequently, the startup stable time at the time of resonator operation is secured and the unnecessary oscillation stable time at the time of external clock supply operation is eliminated to improve the responsiveness.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The oscillator circuit using the resonator for generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit The standby control circuit characterized by having at least the 2nd control circuit which outputs the 2nd control signal for controlling operation of the aforementioned clock generation circuit, and being constituted.
[Claim 2] A reset signal is inputted into a switch terminal and R terminal at the control signal row to which the 1st control circuit of the above is supplied from the outside, respectively. the 1st control signal of the above forms with the flip-flop outputted from Q terminal -- having -- the above -- counting -- with the Schmitt trigger inverter to which a clock generation circuit inputs the oscillation output signal of the aforementioned oscillator circuit into, and outputs the aforementioned perfect clock signal While being formed of the EXOR gate which inputs the output of the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, and a these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock The standby control circuit according to claim 1 in which the 2nd control circuit of the above is formed by the flip-flop by which the 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above is outputted from Q terminal.
[Claim 3] The oscillator circuit using the resonator for generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and

controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit The 2nd control circuit which outputs the 2nd control signal for controlling the reset action of the internal circuitry of the aforementioned semiconductor integrated circuit, The standby control circuit characterized by inputting the reversal signal of the 2nd control signal of the above, and the reset signal supplied from the aforementioned outside, having at least the 3rd control circuit which generates and outputs the internal reset signal to the aforementioned internal circuitry, and being constituted.

[Claim 4] A reset signal is inputted into a switch terminal and R terminal at the control signal row to which the 1st control circuit of the above is supplied from the outside, respectively. the 1st control signal of the above forms with the flip-flop outputted from Q terminal -- having -- the above -- counting -- with the Schmitt trigger inverter to which a clock generation circuit inputs the oscillation output signal of the aforementioned oscillator circuit into, and outputs the aforementioned perfect clock signal While being formed of the EXOR gate which inputs the output of the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, and a these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock While the 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal and the 2nd control circuit of the above is formed by the flip-flop by which the 2nd control signal of the above is outputted from Q terminal The standby control circuit according to claim 3 formed by the flip-flop by which the reset signal to which the 3rd control circuit of the above is supplied from the aforementioned outside is inputted into a switch terminal, the reversal signal of the 2nd control signal of the above is inputted into R terminal, and the 3rd control signal of the above is outputted from Q terminal.

[Claim 5] The oscillator circuit using the resonator for generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit The 2nd control circuit which is controlled by the reset signal supplied to the aforementioned perfect clock signal row from the aforementioned outside, and outputs the 2nd control signal, it controls by the 2nd control signal of the above -- having -- an increment or a decrement -- changing -- operating -- the aforementioned imperfect clock signal -- inputting -- counting, while operating The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit The standby control circuit characterized by having at least the 3rd control circuit which outputs the 3rd control signal for controlling operation of the aforementioned clock generation circuit, and being

constituted.

[Claim 6] A reset signal is inputted into a switch terminal and R terminal at the control signal row to which the 1st control circuit of the above is supplied from the outside, respectively. The 1st control signal of the above is formed by the flip-flop outputted from Q terminal. The reset signal to which the 2nd control circuit of the above is supplied from the aforementioned outside is inputted into R terminal. The aforementioned perfect clock signal is inputted into a switch terminal, and it is formed by the flip-flop by which the 2nd control signal of the above is outputted from Q terminal. the above -- counting -- with the Schmitt trigger inverter to which a clock generation circuit inputs the oscillation output signal of the aforementioned oscillator circuit into, and outputs the aforementioned perfect clock signal While being formed of the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned imperfect clock The standby control circuit according to claim 5 in which the 3rd control circuit of the above is formed by the flip-flop by which the 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above is outputted from Q terminal.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] About a standby control circuit, especially this invention builds in a clock signal generating circuit, and relates to the standby control circuit which controls the inside-and-outside clock signal in a semiconductor integrated circuit.
[0002]
[Description of the Prior Art] In the semiconductor integrated circuit in recently, and the microcomputer formed especially of the semiconductor integrated circuit concerned, the demand which asks for low-power-ization is very strong, and since it corresponds to this, adoption of a CMOS technology is advanced. Moreover, in addition to this CMOS-technology-izing, the original oscillation clock outputted from the oscillator circuit for generating a clock further at the time of standby of a microcomputer is suspended, and the semiconductor integrated circuit which attained minimum-ization of power consumption is developed by forbidding circuit operation of the semiconductor integrated circuit contained in the microcomputer concerned by this.
[0003] Generally a setup of the standby state in these microcomputers is performed by executing a corresponding instruction by the user program, and halt processing of the original oscillation clock by the aforementioned oscillator circuit is performed by the instruction concerned. Moreover, contrary to this, when canceling the standby state of a microcomputer, start processing of a original oscillation is performed by the reset terminal number etc., and execution of a user program is started from the predetermined address. Since a clock will be stabilized at the time of the standup of an oscillator circuit in that case, [whether supply as an internal clock is performed after predetermined-time progress until the oscillation by the oscillator circuit concerned is stabilized, and] Or the counter which had the number of counts corresponding to the aforementioned predetermined time until an oscillation is stabilized set up By canceling internal reset with the overflow signal generated when increment operation is carried out by the oscillation output of a clock and the aforementioned setting number of counts is reached The system is constituted so that the oscillation stable time of a clock oscillator circuit may be secured and program execution may be started with the stable clock.
[0004] Drawing 6 is drawing showing an example of the conventional standby control circuit. The flip prop 18 is set by the stop instruction 112 sent from a microcomputer at the time of standby, and the clock oscillation of an oscillator circuit 19 stops in response to the output of the flip prop 18. Standby release is performed when a flip-flop 18 is reset by the active reset signal 113 from the outside. In response to the output of the set flip-flop 18, the clock oscillation in an oscillator circuit 12 is resumed. And although the internal reset signal 114 outputted from a flip-flop 14 also becomes active simultaneously, reset release to a flip-flop 18 is performed by resetting a flip-flop 14, after the number of counts in the counter 17 of the internal clock signal with which the oscillation output of an

oscillator circuit 19 is outputted through the Schmitt trigger inverter 20 reaches a predetermined value. Therefore, resumption of program execution is begun after the predetermined count time progress in a counter 17, and oscillation judging stable time is secured.

[0005] In such a conventional standby circuit, since it cannot be made to re-operate in the case of the system which operates a microcomputer in response to supply of an external clock, without using a resonator unless it is after the above-mentioned oscillation stable passage of time, the trouble that responsibility is bad intervenes. In order to cope with this trouble, in JP,5-277809,A (Japanese-Patent-Application-No. No. 39650 [three to] official report), the clock signal control circuit is proposed as other conventional examples. In a clock signal control circuit equipped with the oscillator circuit for which the clock signal control circuit by this proposal uses a resonator, and the clock signal generating circuit which generates a clock signal based on the output signal of the oscillator circuit concerned The 1st control circuit which is controlled by the control signal and reset signal from the outside, and controls operation of the aforementioned oscillator circuit, It is initialized by the 1st control circuit of the above, and counting of the output signal of the aforementioned oscillator circuit is carried out. the time of reaching the enumerated data defined beforehand -- counting -- the counting circuit which outputs a signal, and the above -- counting -- it is characterized by having the 2nd control circuit which controls a signal, and the 3rd control circuit which controls operation of the aforementioned clock generation circuit by the above 1st and the 2nd control circuit

[0006] Drawing 7 is drawing showing the example of the clock signal control circuit by the proposal concerned, and is the example applied as a clock signal control circuit of a microcomputer. The flip-flop 22 on which this conventional example functions as an inverter 21 as the 1st control circuit as shown in drawing 7 , The flip-flop 28 which functions as the 2nd control circuit, and the flip-flop 23 which functions as the 3rd control circuit, It has VCO 24 using the resonator, the OR gates 25 and 27, a counter 26, and the clock generation circuit 29, and is constituted. reset of a flip-flop 23 It is set up by the output of a counter 26, and the output of the flip flocks 28 which show operation by the external clock, or operation by the VCO using a resonator beforehand.

[0007] A flip-flop 22 is an RS flip flop, it is set by the stop instruction 102 of a microcomputer, is reset by the active reset signal 103 to which an inverter 21 is reversed and the reset signal 101 of a low level is outputted, and controls operation of VCO 24 by the output. If a counter 26 carries out counting of the oscillation output 104 of VCO 24 and reaches after the fixed passage of time at a predetermined enumerated data, it will output the overflow signal 105. A flip-flop 28 is a power-on flip-flop which is initialized by the power up at logic "0" and is set by execution of a specific instruction. Moreover, a flip-flop 23 is an RS flip flop of set priority, and controls operation of the clock generation circuit 29 in response to the output of a flip-flop 22, and the output of the OR gate 27. And from the clock generation circuit 29, clock signals 106 and 107 are outputted in response to the control signal from the oscillation output 104 and flip-flop 23 of VCO 24.

[0008] Although operation of a flip-flop 28 is controlled by the signal by the instruction of an external signal or a microcomputer etc., in this example, the output signal of a flip-flop 28 is beforehand set as "1" at the time of external clock operation, and is set as "0" at the time of operation by the VCO using a resonator. In standby release operation, like the case of the conventional example of drawing 6 , in resonator operation, the output signal of a flip-flop 28 is set up by "0", if the enumerated data of a counter 26 reaches a predetermined value, a flip-flop 23 will be reset, after oscillation stable time is secured, a clock operates and a program is performed. Moreover, the output of a flip-flop 28 is set as "1" at the time of another side and external clock operation, thereby, since a flip-flop 23 is also reset at the same time it is not concerned with the counted value of a counter 26 at the time of standby release but the reset signal 101 from the outside is canceled, a clock operates and program execution is resumed. Therefore, while the stable time at the time of the standup of VCO 24 using the resonator is

securable, when receiving the clock from the outside, the excessive latency time for oscillation stability shall be deleted, and it does not wait for unnecessary oscillation stable time, and responsibility supposes that it is good.
[0009]
[Problem(s) to be Solved by the Invention] Time is taken for the counter for securing oscillation stable time to operate, in spite of obtaining the clock which was stabilized from the standup point in time in the case of the system which operates a microcomputer in response to supply of an external clock, without using a resonator as an oscillator circuit built in in the conventional standby control circuit mentioned above, and there is a fault that the responsibility at the time of re-operation of the microcomputer concerned falls.
[0010] Moreover, as a method of solving the above-mentioned fault, although JP,4-277809,A (Japanese-Patent-Application-No. No. 39650 [three to] official report) is proposed, in this proposal, the addition of an instruction or addition of a terminal is needed, and there is a fault of causing increase of a circuit scale and increase of cost.
[0011] Moreover, since it is necessary in whether it is resonator operation or it is external clock operation to set up beforehand, there is a fault which lacks in the flexibility in which a corresponding program also must be changed to a system change etc.
[0012]
[Means for Solving the Problem] The oscillator circuit using the resonator for the standby control circuit of the 1st invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit It has at least the 2nd control circuit which outputs the 2nd control signal for controlling operation of the aforementioned clock generation circuit, and is constituted.
[0013] in addition, as the 1st control circuit of the above in the 1st invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively. the flip-flop by which the 1st control signal of the above is outputted from Q terminal -- forming -- the above -- counting -- a clock generation circuit The Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal, While forming by the EXOR gate which inputs the output of the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, and a these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock The 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above may form the 2nd control circuit of the above with the flip-flop outputted from Q terminal.
[0014] Moreover, the oscillator circuit using the resonator for the standby control circuit of the 2nd

invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit The 2nd control circuit which outputs the 2nd control signal for controlling the reset action of the internal circuitry of the aforementioned semiconductor integrated circuit, The reversal signal of the 2nd control signal of the above and the reset signal supplied from the aforementioned outside are inputted, and it has at least the 3rd control circuit which generates and outputs the internal reset signal to the aforementioned internal circuitry, and is constituted.

[0015] In addition, the 1st control circuit of the above in the 2nd invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively. the flip-flop by which the 1st control signal of the above is outputted from Q terminal -- forming -- the above -- counting -- a clock generation circuit The Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal, The inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, It forms by the EXOR gate which inputs the output of these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock. the 2nd control circuit of the above While the 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal and the 2nd control signal of the above forms with the flip-flop outputted from Q terminal The reset signal supplied from the aforementioned outside is inputted into a switch terminal, the reversal signal of the 2nd control signal of the above is inputted into R terminal, and the 3rd control signal of the above may form the 3rd control circuit of the above with the flip-flop outputted from Q terminal.

[0016] Furthermore, the oscillator circuit using the resonator for the standby control circuit of the 3rd invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit The 2nd control circuit which is controlled by the reset signal supplied to the aforementioned perfect clock signal row from the aforementioned outside, and outputs the 2nd control signal, it controls by the 2nd control signal of the above -- having -- an increment or a decrement -- changing -- operating -- the aforementioned imperfect clock signal -- inputting -- counting, while operating The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the

above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit It has at least the 3rd control circuit which outputs the 3rd control signal for controlling operation of the aforementioned clock generation circuit, and is constituted.

[0017] In addition, the 1st control circuit of the above in the 3rd invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively. The 1st control signal of the above forms with the flip-flop outputted from Q terminal. the 2nd control circuit of the above The reset signal supplied from the aforementioned outside is inputted into R terminal, the aforementioned perfect clock signal is inputted into a switch terminal, and it forms with the flip-flop by which the 2nd control signal of the above is outputted from Q terminal. the above -- counting -- a clock generation circuit with the Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal While forming by the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned imperfect clock, the 3rd control circuit of the above The 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above may form with the flip-flop outputted from Q terminal.

[0018]

[Example] Next, this invention is explained with reference to a drawing.

[0019] Drawing 1 is the block diagram showing the 1st example of this invention. counting in which this example includes flip-flops 1 and 5, an oscillator circuit 2, the Schmitt trigger inverter 31 and an inverter 32, and the EXOR gate 33 as shown in drawing 1 -- it has the clock generation circuit 3, a counter 4, the clock generation circuit 6, and OR circuit 7, and is constituted

[0020] in drawing 1 , a flip-flop 1 is an RS flip flop, and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted is sent to an oscillator circuit 2, and motion control to the oscillator circuit concerned is performed In addition, while the flip-flop 1 is set, the signal 103 of a low level is outputted as the output. in response to the signal 103 of "0" outputted from the flip-flop 2 concerned, an oscillator circuit 2 will be in an oscillation state, and the oscillation signal 104 will output from the oscillator circuit 2 concerned -- having -- counting -- it is inputted into the clock generation circuit 3 and clock generation ****** 6 The clock generation circuit 3 is formed of the Schmitt trigger inverter 31, the normal type inverter 32 without a hysteresis characteristic, and the EXOR gate 33 of 2 inputs. counting -- [when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level] In being the clock of amplitude level with the inadequate oscillation signal 104 which the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31, and is outputted from an oscillator circuit 2 The imperfect clock 106 is outputted through the EXOR gate 33 of the output of the Schmitt trigger inverter 31 and the normal inverter 32.

[0021] a counter 4 -- counting -- it is the up / down counter which carries out decrement operation with the perfect clock 105 outputted from the clock generation circuit 3, and carries out increment operation with the imperfect clock 106, and the underflow signal (henceforth a UDF signal) 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, and in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4, a signal 108 is outputted and it is inputted into the clock generation circuit 6 and the OR gate 7. While operation of the clock generation circuit 6 is controlled through this signal 108, reset of a counter 4 is controlled. In the clock generation circuit 6, the clock signal 104 outputted from an oscillator circuit 2 is inputted, and the ******** predetermined clock signals 109 and 110 are generated and outputted also to the clock signal

concerned.

[0022] Drawing 2 (a), (b), (c), (d), (e), (f), (g), and (h) It is the timing chart showing the signal of each part at the time of using the resonator of this example. moreover, drawing 3 (a), (b), (c), (d), (e), (f), (g), and (h) It is the timing chart showing the signal of each part in the case of receiving supply of a clock pulse from the exterior of this example.

[0023] Next, operation when drawing 1 and drawing 2 use the resonator of this example with reference to the beginning is explained. First, time T0 If it sets, a power supply is switched on and a reset signal 101 (refer to drawing 2 (a)) is set to "1", a flip-flop 1 and a counter 4, the internal circuitry in the semiconductor integrated circuit concerned, etc. will be initialized. Moreover, although the signal 108 (refer to drawing 2 (g)) outputted from a flip-flop 5 is satisfactory since the reset signal 101 of a power up is "1" between usually sufficient time for the stability of an oscillation even if "0" or "1" is any, it shall be "1" for convenience here. Therefore, since the signal 108 inputted into the clock generation circuit 6 is "1" even if an oscillator circuit 2 is in an oscillation state, the clock generation circuit 6 is in a idle state. Moreover, since the signal 103 (refer to drawing 2 (b)) outputted from a flip-flop 1 is "0", an oscillator circuit 2 starts an oscillation and the amplitude level of the oscillation signal 104 (refer to drawing 2 (c)) outputted from the oscillator circuit 2 concerned turns into large level gradually. Subsequently, time T1 Although it sets and a reset signal 101 is set to "0", since the signal 108 outputted from a flip-flop 5 is "1", clock signals 109 and 110 are not outputted from the clock generation circuit 6. Although reset is canceled and a counter is started in a counter 4 Since the amplitude of the oscillation signal 104 outputted from an oscillator circuit 2 is small, the Schmitt trigger inverter 31 does not induce this. In order that a clock signal will be transmitted only from the normal inverter 32, the perfect clock signal 105 (refer to drawing 2 (d)) will be in a idle state and only the imperfect clock 106 (refer to drawing 2 (e)) may operate, in response in a counter 4, increment operation is performed.

[0024] Time T2 It sets and the amplitude level of a clock signal 104 grows, if the predetermined level which the Schmitt trigger inverter 31 induces is reached, the imperfect clock 105 will stop and operation of the perfect clock 106 will be started. Therefore, in a counter 4, the operation shifts to decrement operation from increment operation. And time T3 If it sets, a counter 4 carries out an underflow and the UDF signal 107 is outputted, in response, a flip-flop 5 will be reset and the clock generation circuit 6 will be in operating state through the signal 108 of "1" outputted from a flip-flop 5, and in response to the oscillation signal 104, from the clock generation circuit 6 concerned, clock signals 109 and 110 will be outputted and it will be sent out to the internal circuitry in a semiconductor integrated circuit. And time T4 If it sets and the stop signal 102 (refer to drawing 2 (h)) from the outside is inputted While both the flip-flops 1 and 5 are set in response, the oscillation of an oscillator circuit 2 stops in response to the signal 103 of "1" outputted from a flip-flop 1 and a counter 4 is initialized In response to the signal 108 of "1" outputted from a flip-flop 5, the output of the clock signals 109 and 110 from the clock generation circuit 6 is also suspended. For this reason, the power consumption in a semiconductor integrated circuit will be in the minimum state.

[0025] And by setting a reset signal 101 to "1" again, the oscillation of an oscillator circuit 2 is started through the output 103 of the FURIFFUFU rope 1, and a counter 4 is initialized through the OR gate 7. setting a reset signal 101 to "0" -- a counter 4 -- the period when the amplitude level of the oscillation signal 104 is inadequate as mentioned above -- setting -- counting -- decrement operation is performed by the perfect clock 106, after increment operation being performed by the imperfect clock 105 outputted from the clock generation circuit 3 and reaching predetermined amplitude level Moreover, rather than the clock generation circuit 6, the output of clock signals 109 and 110 is resumed through the output 108 of a flip-flop 5 by setting counter 4, and generating and outputting the UDF signal 107. That is, the amplitude level of the oscillation signal 104 outputted from an oscillator

circuit 3 becomes possible [securing the oscillation stable time according to time until it reaches predetermined level].

[0026] Next, with reference to drawing 1 and drawing 3 , operation of this example in the case of receiving supply of a clock pulse from the exterior is explained. In addition, in here, explanation shall be omitted about the point which overlaps operation of this example at the time of using the above-mentioned resonator, and a different point from operation shown in the timing chart of above-mentioned drawing 2 (a), (b), (c), (d), (e), (f), (g), and (h) shall be explained. Since it is in the state of receiving supply of the clock from the outside, the oscillation signal 104 (refer to drawing 3 (c)) outputted from the oscillator circuit 2 in drawing 1 is time T0. It sets, and shortly after the reset signal 101 (refer to drawing 3 (a)) inputted into a flip-flop 1 becomes active, in response to the signal 103 (refer to drawing 3 (b)) of "0" outputted from the flip-flop 1 concerned, an oscillation is started on sufficient amplitude level. Therefore, a clock signal is transmitted similarly from the Schmitt trigger inverter 31 and the normal inverter 32, the perfect clock 105 (refer to drawing 3 (d)) will be in operating state, it will be outputted, and the imperfect clock 106 (refer to drawing 3 (e)) will be in a idle state. It corresponds to this and is time T1. If it sets and a counter 4 has reset canceled, decrement operation will be performed, and rather than a counter 4, the UDF signal 107 (refer to drawing 3 (f)) is outputted after 1 clock, and it is inputted into a flip-flop 5. In a flip-flop 5, it is reset by the reset terminal in response to this UDF signal 107, and the output 108 (refer to drawing 3 (g)) is inputted into the clock generation circuit 6. The clock generation circuit 6 will be in operating state in response to the signal 108 of "0" outputted from a flip-flop 5, clock signals 109 and 110 are outputted corresponding to the input of the oscillation signal 104 from an oscillator circuit 2, it is sent to the internal circuitry in a semiconductor integrated circuit, and operation of the internal circuitry concerned is started.

[0027] Time T4 If it sets and a stop signal 102 (refer to drawing 3 (h)) is inputted, both the flip-flops 1 and 5 will be set, and the oscillation of an oscillator circuit 2 will stop in response to the signal 103 of "1" outputted from a flip-flop 1's by this. Moreover, the output of the clock signals 109 and 110 corresponding to [while a counter 3 is initialized through a signal 108, operation of the clock generation circuit 6 is stopped, and] the input of the oscillation signal 104 from an oscillator circuit 2 of "1" outputted through a flip-flop 5 is also suspended. For this reason, in this state, the power consumption in a semiconductor integrated circuit serves as the minimum. And again, if a reset signal 101 is set as "1", an oscillator circuit 2 will start an oscillation and, thereby, a counter 4 will be initialized. Moreover, when a reset signal 101 is set as "0", since the amplitude of the clock 104 with which a counter 4 is outputted from an oscillator circuit 2 is sufficient level, increment operation with the imperfect clock 106 is not performed, but decrement operation with the perfect clock 105 is performed immediately. Moreover, by the UDF signal's 107 occurring and outputting it in a counter 4, in this case, the signal 108 outputted from a flip-flop 5 is set to "0", thereby, the clock generation circuit 6 will be in operating state, and sending out of the clock signals 109 and 110 to the internal circuitry of a semiconductor integrated circuit is resumed. That is, since the amplitude level of the oscillation signal 104 outputted from an oscillator circuit 2 has reached predetermined level from the start, operation of a semiconductor integrated circuit can be made to start without oscillation stable time.

[0028] Next, the 2nd example of this invention is explained. Drawing 4 is the block diagram showing the composition of this example. it is shown in drawing 4 -- as -- this example -- flip-flops 1, 5, and 9, an oscillator circuit 2, and counting -- the clock generation circuit 3, a counter 4, the clock generation circuit 8, OR circuit 7, and an inverter 10 are had and constituted -- having -- **** -- counting -- the composition of the clock generation circuit 3 is the same as that of the case of the 1st example shown

in drawing 1 , and is formed of the Schmitt trigger inverter 31, the normal type inverter 32, and the EXOR gate The constitutional difference with the 1st example of this example is that the flip-flop 9 and the inverter 10 are newly added.

[0029] in drawing 4 , a flip-flop 1 is an RS flip flop, and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted from the flip-flop 1 concerned is sent to an oscillator circuit 2, and motion control to an oscillator circuit 2 is performed In this case, while the flip-flop 1 concerned is reset, it is outputted as a signal, and the signal 103 outputted from a flip-flop 1 is outputted as a signal of "1", while ["0"] being set. While the flip-flop 1 is reset in the oscillator circuit 2 in response (a signal 103 is "0"), it will be in an oscillation state and the oscillation signal 104 is outputted, and while the flip-flop 1 is set (a signal 103 is "1"), the signal of a low level is outputted.

[0030] The clock generation circuit 3 is formed of the Schmitt trigger inverter 31, the normal type inverter 32 without a hysteresis characteristic, and the EXOR gate 33 of 2 inputs. counting -- [when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level] In being the clock of amplitude level with the inadequate oscillation signal 104 which the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31, and is outputted from an oscillator circuit 2 The output of the Schmitt trigger inverter 31 and the normal type inverter 32 is outputted as an imperfect clock 106 through the EXOR gate 33.

[0031] a counter 4 -- counting -- it is the up / down counter which carries out decrement operation with the perfect clock 105 outputted from the clock generation circuit 3, and carries out increment operation with the imperfect clock 106, and the UDF signal 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, is inputted into a flip-flop 9 through an inverter 10, and functions as an object for control of an internal reset signal while a signal 108 is outputted and being inputted into a counter 4 through the OR gate 7 in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4. Moreover, in the clock generation circuit 8, the oscillation signal 104 outputted from an oscillator circuit 2 is inputted, the ******** predetermined clock signals 109 and 110 are generated and outputted also to the oscillation signal 104 concerned, and it is sent out to the internal circuitry of a semiconductor integrated circuit. And the newly added flip-flop 9 is an RS flip flop of set priority, and in response to the input of the signal with which the signal 108 outputted from a flip-flop 5 was reversed by the inverter 10, and a reset signal 101, a reset signal 114 is generated and outputted and it is sent out to the internal circuitry of a semiconductor integrated circuit.

[0032] The difference between this example and the 1st above-mentioned example As opposed to operation of the clock generation circuit 6 being controlled by the signal 108 outputted from a flip-flop 5 in the 1st example In the clock generation circuit 8 in this example Corresponding to the input of the oscillation signal 104 outputted from an oscillator circuit 2, it is constituted so that the ** clock signals 109 and 110 may be outputted. In the limitation as which the oscillation signal 104 concerned is inputted, I hear that the ****** clock signals 109 and 110 are outputted from the clock generation circuit 8 to an internal circuitry, and there are.

[0033] Moreover, other differences with the 1st example of this example As a reset signal to the internal circuitry of the semiconductor integrated circuit in the 1st example A reset signal 101 sets to this example to being directly sent out to the internal circuitry concerned as it is. The reset signal 114 to the internal circuitry of a semiconductor integrated circuit is using the signal outputted from a flip-flop 9 as the reset signal 114 concerned through the reversal signal of the output 108 of the flip-flop 5 set in response to the input of a reset signal 101.

[0034] Therefore, in the 1st example mentioned above, after oscillation stable time is secured, clock signals 109 and 110 are outputted, and it contrasts with operation in the internal circuitry of a

semiconductor integrated circuit being started. In this example, corresponding to an oscillator circuit 2 operating, it begins and the shell clock signals 109 and 110 are generated, after oscillation stable time is secured, an internal reset signal is canceled, and operation in the internal circuitry of a semiconductor integrated circuit is started. However, about the point that operation of an internal circuitry is started after the oscillation stable passage of time in the case of which [of the above 1st and the 2nd example], it is the same.

[0035] Moreover, when operating with the clock from the outside, without using a resonator, in the case of this example, in the state where there is no oscillation stable time like the case of the 1st above-mentioned example, it is not necessary to say that an internal reset signal is canceled and operation of the internal circuitry of a semiconductor integrated circuit is started immediately.

[0036] Next, the 3rd example of this invention is explained. Drawing 5 is the block diagram showing the composition of this example. counting in which this example contains flip-flops 1, 5, and 12, an oscillator circuit 2, and the Schmitt trigger inverter 31 and the normal type inverter 32 as shown in drawing 5 -- it has the clock generation circuit 11, a counter 13, the clock generation circuit 6, and the OR gate 7, and is constituted the constitutional difference with the 1st example of this example -- counting -- it is in the content of composition containing the clock generation circuit 11, a flip-flop 12, and a counter 13

[0037] in drawing 5 , like the case of the 1st and 2nd examples, a flip-flop 1 is an RS flip flop of set priority, and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted from the flip-flop 1 concerned is sent to an oscillator circuit 2, and motion control to an oscillator circuit 2 is performed In this case, the signal 103 outputted from a flip-flop 1 is outputted as a signal of "0", while the flip-flop 1 concerned is reset. Moreover, while being set, in response, it sets in the point of "1" outputted as a signal, and a row at an oscillator circuit 2. While the flip-flop 1 is reset (a signal 103 is "0"), will be in an oscillation state and the oscillation signal 104 will be outputted. It is the same as that of the case of the above-mentioned 1st and the 2nd example that the signal of a low level is outputted while the flip-flop 1 is set (a signal 103 is "1").

[0038] counting -- the amplitude level of the oscillation signal 104 which the clock generation circuit 11 is formed of the Schmitt trigger inverter 31 and the normal type inverter 32 without a hysteresis characteristic, the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31 when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level, and is outputted from an oscillator circuit 2 is not related how, but the imperfect clock 111 is outputted through the normal inverter 32 a counter 4 -- counting -- counter operation is carried out with the imperfect clock 111 outputted from the clock generation circuit 11, it is in the up / down counter which changes to any of an increment or a decrement they are, and operates in response to the signal outputted from a flip-flop 12, and the UDF signal 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, and in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4, a signal 108 is outputted and it is inputted into the clock generation circuit 6 and the OR gate 7. While operation of the clock generation circuit 6 is controlled through this signal 108, reset of a counter 4 is controlled through the OR gate 7. In the clock generation circuit 6, the oscillation signal 104 outputted from an oscillator circuit 2 is inputted, and the predetermined clock signals 109 and 110 are generated and outputted based on the oscillation signal concerned.

[0039] In the 1st example mentioned above, the decrement of the counter 4 was carried out with the perfect clock 105 which increments a counter 4 with the imperfect clock 106 generated when the amplitude level of the oscillation signal 104 outputted from an oscillator circuit 2 is small, and is generated when amplitude level is sufficient level, and the underflow is detected. counting [as

opposed to the direct counter 13 for the imperfect clock 111 which the amplitude level of the oscillation signal 104 is not related how, but is generated in this example as contrasted with this] -- it uses as a clock and the increment in a counter 13 is performed And when it sets after that and the amplitude level of a clock becomes large enough, in the standup of the perfect clock 105 which starts operation, the mode of operation in a counter 13 was changed from the increment to the decrement, and the underflow is detected. In operating by supply of an external clock like the case of the 1st example in the case of this example, in order to go into decrement operation, without performing increment operation in a counter 13 in order that the perfect clock 105 may operate immediately, oscillation stable time is deleted.

[0040]

[Effect of the Invention] As explained above, this invention is effective in the ability to eliminate the useless latency time for oscillation stability, and raise responsibility, when operating by clock supply from the outside, while the stable time at the time of the standup of the oscillator circuit at the time of using a resonator is secured.

[0041] Moreover, the effect that a system can be built is in a program row by recognizing whether the standby circuit itself is operation using the resonator, or it is operation by external clock supply, without being conscious of the method of clock supply as a user.

[0042] Furthermore, in this invention, stable time is shortened so automatically that a standup is quick, and since stable time is set up for a long time so automatically that a standup is late, it is effective in the stable time which was adapted for the build up time which changes with the ambient conditions by the temperature of a resonator etc. being secured.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] About a standby control circuit, especially this invention builds in a clock signal generating circuit, and relates to the standby control circuit which controls the inside-and-outside clock signal in a semiconductor integrated circuit.

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PRIOR ART

[Description of the Prior Art] In the semiconductor integrated circuit in recently, and the microcomputer formed especially of the semiconductor integrated circuit concerned, the demand which asks for low-power-ization is very strong, and since it corresponds to this, adoption of a CMOS technology is advanced. Moreover, in addition to this CMOS-technology-izing, the original oscillation clock outputted from the oscillator circuit for generating a clock further at the time of standby of a microcomputer is suspended, and the semiconductor integrated circuit which attained minimum-ization of power consumption is developed by forbidding circuit operation of the semiconductor integrated circuit contained in the microcomputer concerned by this.
[0003] Generally a setup of the standby state in these microcomputers is performed by executing a corresponding instruction by the user program, and halt processing of the original oscillation clock by the aforementioned oscillator circuit is performed by the instruction concerned. Moreover, contrary to this, when canceling the standby state of a microcomputer, start processing of a original oscillation is performed by the reset terminal number etc., and execution of a user program is started from the predetermined address. Since a clock will be stabilized at the time of the standup of an oscillator circuit in that case, [whether supply as an internal clock is performed after predetermined-time progress until the oscillation by the oscillator circuit concerned is stabilized, and] Or the counter which had the number of counts corresponding to the aforementioned predetermined time until an oscillation is stabilized set up By canceling internal reset with the overflow signal generated when increment operation is carried out by the oscillation output of a clock and the aforementioned setting number of counts is reached The system is constituted so that the oscillation stable time of a clock oscillator circuit may be secured and program execution may be started with the stable clock.
[0004] Drawing 6 is drawing showing an example of the conventional standby control circuit. The flip prop 18 is set by the stop instruction 112 sent from a microcomputer at the time of standby, and the clock oscillation of an oscillator circuit 19 stops in response to the output of the flip prop 18. Standby release is performed when a flip-flop 18 is reset by the active reset signal 113 from the outside. In response to the output of the set flip-flop 18, the clock oscillation in an oscillator circuit 12 is resumed. And although the internal reset signal 114 outputted from a flip-flop 14 also becomes active simultaneously, reset release to a flip-flop 18 is performed by resetting a flip-flop 14, after the number of counts in the counter 17 of the internal clock signal with which the oscillation output of an oscillator circuit 19 is outputted through the Schmitt trigger inverter 20 reaches a predetermined value. Therefore, resumption of program execution is begun after the predetermined count time progress in a counter 17, and oscillation judging stable time is secured.
[0005] In such a conventional standby circuit, since it cannot be made to re-operate in the case of the system which operates a microcomputer in response to supply of an external clock, without using a resonator unless it is after the above-mentioned oscillation stable passage of time, the trouble that

responsibility is bad intervenes. In order to cope with this trouble, in JP,5-277809,A (Japanese-Patent-Application-No. No. 39650 [three to] official report), the clock signal control circuit is proposed as other conventional examples. In a clock signal control circuit equipped with the oscillator circuit for which the clock signal control circuit by this proposal uses a resonator, and the clock signal generating circuit which generates a clock signal based on the output signal of the oscillator circuit concerned The 1st control circuit which is controlled by the control signal and reset signal from the outside, and controls operation of the aforementioned oscillator circuit, It is initialized by the 1st control circuit of the above, and counting of the output signal of the aforementioned oscillator circuit is carried out. the time of reaching the enumerated data defined beforehand -- counting -- the counting circuit which outputs a signal, and the above -- counting -- it is characterized by having the 2nd control circuit which controls a signal, and the 3rd control circuit which controls operation of the aforementioned clock generation circuit by the above 1st and the 2nd control circuit

[0006] Drawing 7 is drawing showing the example of the clock signal control circuit by the proposal concerned, and is the example applied as a clock signal control circuit of a microcomputer. The flip-flop 22 on which this conventional example functions as an inverter 21 as the 1st control circuit as shown in drawing 7 , The flip-flop 28 which functions as the 2nd control circuit, and the flip-flop 23 which functions as the 3rd control circuit, It has VCO 24 using the resonator, the OR gates 25 and 27, a counter 26, and the clock generation circuit 29, and is constituted. reset of a flip-flop 23 It is set up by the output of a counter 26, and the output of the flip flocks 28 which show operation by the external clock, or operation by the VCO using a resonator beforehand.

[0007] A flip-flop 22 is an RS flip flop, it is set by the stop instruction 102 of a microcomputer, is reset by the active reset signal 103 to which an inverter 21 is reversed and the reset signal 101 of a low level is outputted, and controls operation of VCO 24 by the output. If a counter 26 carries out counting of the oscillation output 104 of VCO 24 and reaches after the fixed passage of time at a predetermined enumerated data, it will output the overflow signal 105. A flip-flop 28 is a power-on flip-flop which is initialized by the power up at logic "0" and is set by execution of a specific instruction. Moreover, a flip-flop 23 is an RS flip flop of set priority, and controls operation of the clock generation circuit 29 in response to the output of a flip-flop 22, and the output of the OR gate 27. And from the clock generation circuit 29, clock signals 106 and 107 are outputted in response to the control signal from the oscillation output 104 and flip-flop 23 of VCO 24.

[0008] Although operation of a flip-flop 28 is controlled by the signal by the instruction of an external signal or a microcomputer etc., in this example, the output signal of a flip-flop 28 is beforehand set as "1" at the time of external clock operation, and is set as "0" at the time of operation by the VCO using a resonator. In standby release operation, like the case of the conventional example of drawing 6 , in resonator operation, the output signal of a flip-flop 28 is set up by "0", if the enumerated data of a counter 26 reaches a predetermined value, a flip-flop 23 will be reset, after oscillation stable time is secured, a clock operates and a program is performed. Moreover, the output of a flip-flop 28 is set as "1" at the time of another side and external clock operation, thereby, since a flip-flop 23 is also reset at the same time it is not concerned with the counted value of a counter 26 at the time of standby release but the reset signal 101 from the outside is canceled, a clock operates and program execution is resumed. Therefore, while the stable time at the time of the standup of VCO 24 using the resonator is securable, when receiving the clock from the outside, the excessive latency time for oscillation stability shall be deleted, and it does not wait for unnecessary oscillation stable time, and responsibility supposes that it is good.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, this invention is effective in the ability to eliminate the useless latency time for oscillation stability, and raise responsibility, when operating by clock supply from the outside, while the stable time at the time of the standup of the oscillator circuit at the time of using a resonator is secured.
[0041] Moreover, the effect that a system can be built is in a program row by recognizing whether the standby circuit itself is operation using the resonator, or it is operation by external clock supply, without being conscious of the method of clock supply as a user.
[0042] Furthermore, in this invention, stable time is shortened so automatically that a standup is quick, and since stable time is set up for a long time so automatically that a standup is late, it is effective in the stable time which was adapted for the build up time which changes with the ambient conditions by the temperature of a resonator etc. being secured.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Time is taken for the counter for securing oscillation stable time to operate, in spite of obtaining the clock which was stabilized from the standup point in time in the case of the system which operates a microcomputer in response to supply of an external clock, without using a resonator as an oscillator circuit built in in the conventional standby control circuit mentioned above, and there is a fault that the responsibility at the time of re-operation of the microcomputer concerned falls.

[0010] Moreover, as a method of solving the above-mentioned fault, although JP,4-277809,A (Japanese-Patent-Application-No. No. 39650 [three to] official report) is proposed, in this proposal, the addition of an instruction or addition of a terminal is needed, and there is a fault of causing increase of a circuit scale and increase of cost.

[0011] Moreover, since it is necessary in whether it is resonator operation or it is external clock operation to set up beforehand, there is a fault which lacks in the flexibility in which a corresponding program also must be changed to a system change etc.

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MEANS

[Means for Solving the Problem] The oscillator circuit using the resonator for the standby control circuit of the 1st invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit It has at least the 2nd control circuit which outputs the 2nd control signal for controlling operation of the aforementioned clock generation circuit, and is constituted.
[0013] in addition, as the 1st control circuit of the above in the 1st invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively. the flip-flop by which the 1st control signal of the above is outputted from Q terminal -- forming -- the above -- counting -- a clock generation circuit The Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal, While forming by the EXOR gate which inputs the output of the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, and a these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock The 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above may form the 2nd control circuit of the above with the flip-flop outputted from Q terminal.
[0014] Moreover, the oscillator circuit using the resonator for the standby control circuit of the 2nd invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the

aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit While inputting an imperfect clock signal into the aforementioned perfect clock signal row, the aforementioned perfect clock signal's performing decrement operation and the aforementioned imperfect clock signal's performing increment operation The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit The 2nd control circuit which outputs the 2nd control signal for controlling the reset action of the internal circuitry of the aforementioned semiconductor integrated circuit, The reversal signal of the 2nd control signal of the above and the reset signal supplied from the aforementioned outside are inputted, and it has at least the 3rd control circuit which generates and outputs the internal reset signal to the aforementioned internal circuitry, and is constituted.

[0015] In addition, the 1st control circuit of the above in the 2nd invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively. the flip-flop by which the 1st control signal of the above is outputted from Q terminal -- forming -- the above -- counting -- a clock generation circuit The Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal, The inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, reverses, and is outputted, It forms by the EXOR gate which inputs the output of these Schmitt trigger inverters and an inverter, and outputs the aforementioned imperfect clock. the 2nd control circuit of the above While the 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal and the 2nd control signal of the above forms with the flip-flop outputted from Q terminal The reset signal supplied from the aforementioned outside is inputted into a switch terminal, the reversal signal of the 2nd control signal of the above is inputted into R terminal, and the 3rd control signal of the above may form the 3rd control circuit of the above with the flip-flop outputted from Q terminal.

[0016] Furthermore, the oscillator circuit using the resonator for the standby control circuit of the 3rd invention generating the clock signal supplied to the internal circuitry in a semiconductor integrated circuit, In a standby control circuit including the clock generation circuit which generates the aforementioned clock signal based on the oscillation output signal of the oscillator circuit concerned The 1st control circuit which outputs the 1st control signal for being controlled by the reset signal by the control signal row supplied from the outside, and controlling operation of the aforementioned oscillator circuit, counting which detects the amplitude level of the oscillation output signal of the aforementioned oscillator circuit, dissociates, respectively, and generates and outputs the perfect clock signal and imperfect clock signal corresponding to the amplitude level concerned -- with a clock generation circuit The 2nd control circuit which is controlled by the reset signal supplied to the aforementioned perfect clock signal row from the aforementioned outside, and outputs the 2nd control signal, it controls by the 2nd control signal of the above -- having -- an increment or a decrement -- changing -- operating -- the aforementioned imperfect clock signal -- inputting -- counting, while operating The counting circuit which outputs an underflow signal corresponding to a predetermined enumerated data, While inputting the 1st control signal outputted from the 1st control circuit of the above, and the underflow signal outputted from the aforementioned counting circuit and controlling initialization of the aforementioned counting circuit It has at least the 3rd control circuit which outputs the 3rd control signal for controlling operation of the aforementioned clock generation circuit, and is constituted.

[0017] In addition, the 1st control circuit of the above in the 3rd invention A reset signal is inputted into a switch terminal and R terminal at the control signal row supplied from the outside, respectively.

The 1st control signal of the above forms with the flip-flop outputted from Q terminal. the 2nd control circuit of the above The reset signal supplied from the aforementioned outside is inputted into R terminal, the aforementioned perfect clock signal is inputted into a switch terminal, and it forms with the flip-flop by which the 2nd control signal of the above is outputted from Q terminal. the above -- counting -- a clock generation circuit with the Schmitt trigger inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned perfect clock signal While forming by the inverter which inputs the oscillation output signal of the aforementioned oscillator circuit, and outputs the aforementioned imperfect clock, the 3rd control circuit of the above The 1st control signal of the above is inputted into a switch terminal, the aforementioned underflow signal is inputted into R terminal, and the 2nd control signal of the above may form with the flip-flop outputted from Q terminal.

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EXAMPLE

[Example] Next, this invention is explained with reference to a drawing.
[0019] Drawing 1 is the block diagram showing the 1st example of this invention. counting in which this example includes flip-flops 1 and 5, an oscillator circuit 2, the Schmitt trigger inverter 31 and an inverter 32, and the EXOR gate 33 as shown in drawing 1 -- it has the clock generation circuit 3, a counter 4, the clock generation circuit 6, and OR circuit 7, and is constituted
[0020] in drawing 1 , a flip-flop 1 is an RS flip flop, and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted is sent to an oscillator circuit 2, and motion control to the oscillator circuit concerned is performed In addition, while the flip-flop 1 is set, the signal 103 of a low level is outputted as the output. in response to the signal 103 of "0" outputted from the flip-flop 2 concerned, an oscillator circuit 2 will be in an oscillation state, and the oscillation signal 104 will output from the oscillator circuit 2 concerned -- having -- counting -- it is inputted into the clock generation circuit 3 and clock generation ****** 6 The clock generation circuit 3 is formed of the Schmitt trigger inverter 31, the normal type inverter 32 without a hysteresis characteristic, and the EXOR gate 33 of 2 inputs. counting -- [when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level] In being the clock of amplitude level with the inadequate oscillation signal 104 which the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31, and is outputted from an oscillator circuit 2 The imperfect clock 106 is outputted through the EXOR gate 33 of the output of the Schmitt trigger inverter 31 and the normal inverter 32.
[0021] a counter 4 -- counting -- it is the up / down counter which carries out decrement operation with the perfect clock 105 outputted from the clock generation circuit 3, and carries out increment operation with the imperfect clock 106, and the underflow signal (henceforth a UDF signal) 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, and in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4, a signal 108 is outputted and it is inputted into the clock generation circuit 6 and the OR gate 7. While operation of the clock generation circuit 6 is controlled through this signal 108, reset of a counter 4 is controlled. In the clock generation circuit 6, the clock signal 104 outputted from an oscillator circuit 2 is inputted, and the ******** predetermined clock signals 109 and 110 are generated and outputted also to the clock signal concerned.
[0022] Drawing 2 (a), (b), (c), (d), (e), (f), (g), and (h) It is the timing chart showing the signal of each part at the time of using the resonator of this example. moreover, drawing 3 (a), (b), (c), (d), (e), (f), (g), and (h) It is the timing chart showing the signal of each part in the case of receiving supply of a clock pulse from the exterior of this example.
[0023] Next, operation when drawing 1 and drawing 2 use the resonator of this example with

reference to the beginning is explained. First, time T0 If it sets, a power supply is switched on and a reset signal 101 (refer to drawing 2 (a)) is set to "1", a flip-flop 1 and a counter 4, the internal circuitry in the semiconductor integrated circuit concerned, etc. will be initialized. Moreover, although the signal 108 (refer to drawing 2 (g)) outputted from a flip-flop 5 is satisfactory since the reset signal 101 of a power up is "1" between usually sufficient time for the stability of an oscillation even if "0" or "1" is any, it shall be "1" for convenience here. Therefore, since the signal 108 inputted into the clock generation circuit 6 is "1" even if an oscillator circuit 2 is in an oscillation state, the clock generation circuit 6 is in a idle state. Moreover, since the signal 103 (refer to drawing 2 (b)) outputted from a flip-flop 1 is "0", an oscillator circuit 2 starts an oscillation and the amplitude level of the oscillation signal 104 (refer to drawing 2 (c)) outputted from the oscillator circuit 2 concerned turns into large level gradually. Subsequently, time T1 Although it sets and a reset signal 101 is set to "0", since the signal 108 outputted from a flip-flop 5 is "1", clock signals 109 and 110 are not outputted from the clock generation circuit 6. Although reset is canceled and a counter is started in a counter 4 Since the amplitude of the oscillation signal 104 outputted from an oscillator circuit 2 is small, the Schmitt trigger inverter 31 does not induce this. In order that a clock signal will be transmitted only from the normal inverter 32, the perfect clock signal 105 (refer to drawing 2 (d)) will be in a idle state and only the imperfect clock 106 (refer to drawing 2 (e)) may operate, in response in a counter 4, increment operation is performed.

[0024] Time T2 It sets and the amplitude level of a clock signal 104 grows, if the predetermined level which the Schmitt trigger inverter 31 induces is reached, the imperfect clock 105 will stop and operation of the perfect clock 106 will be started. Therefore, in a counter 4, the operation shifts to decrement operation from increment operation. And time T3 If it sets, a counter 4 carries out an underflow and the UDF signal 107 is outputted, in response, a flip-flop 5 will be reset and the clock generation circuit 6 will be in operating state through the signal 108 of "1" outputted from a flip-flop 5, and in response to the oscillation signal 104, from the clock generation circuit 6 concerned, clock signals 109 and 110 will be outputted and it will be sent out to the internal circuitry in a semiconductor integrated circuit. And time T4 If it sets and the stop signal 102 (refer to drawing 2 (h)) from the outside is inputted While both the flip-flops 1 and 5 are set in response, the oscillation of an oscillator circuit 2 stops in response to the signal 103 of "1" outputted from a flip-flop 1 and a counter 4 is initialized In response to the signal 108 of "1" outputted from a flip-flop 5, the output of the clock signals 109 and 110 from the clock generation circuit 6 is also suspended. For this reason, the power consumption in a semiconductor integrated circuit will be in the minimum state.

[0025] And by setting a reset signal 101 to "1" again, the oscillation of an oscillator circuit 2 is started through the output 103 of the FURIFFUFU rope 1, and a counter 4 is initialized through the OR gate 7. setting a reset signal 101 to "0" -- a counter 4 -- the period when the amplitude level of the oscillation signal 104 is inadequate as mentioned above -- setting -- counting -- decrement operation is performed by the perfect clock 106, after increment operation being performed by the imperfect clock 105 outputted from the clock generation circuit 3 and reaching predetermined amplitude level Moreover, rather than the clock generation circuit 6, the output of clock signals 109 and 110 is resumed through the output 108 of a flip-flop 5 by setting counter 4, and generating and outputting the UDF signal 107. That is, the amplitude level of the oscillation signal 104 outputted from an oscillator circuit 3 becomes possible [securing the oscillation stable time according to time until it reaches predetermined level].

[0026] Next, with reference to drawing 1 and drawing 3 , operation of this example in the case of receiving supply of a clock pulse from the exterior is explained. In addition, in here, explanation shall be omitted about the point which overlaps operation of this example at the time of using the above-mentioned resonator, and a different point from operation shown in the timing chart of

above-mentioned drawing 2 (a), (b), (c), (d), (e), (f), (g), and (h) shall be explained. Since it is in the state of receiving supply of the clock from the outside, the oscillation signal 104 (refer to drawing 3 (c)) outputted from the oscillator circuit 2 in drawing 1 is time T0. It sets, and shortly after the reset signal 101 (refer to drawing 3 (a)) inputted into a flip-flop 1 becomes active, in response to the signal 103 (refer to drawing 3 (b)) of "0" outputted from the flip-flop 1 concerned, an oscillation is started on sufficient amplitude level. Therefore, a clock signal is transmitted similarly from the Schmitt trigger inverter 31 and the normal inverter 32, the perfect clock 105 (refer to drawing 3 (d)) will be in operating state, it will be outputted, and the imperfect clock 106 (refer to drawing 3 (e)) will be in a idle state. It corresponds to this and is time T1. If it sets and a counter 4 has reset canceled, decrement operation will be performed, and rather than a counter 4, the UDF signal 107 (refer to drawing 3 (f)) is outputted after 1 clock, and it is inputted into a flip-flop 5. In a flip-flop 5, it is reset by the reset terminal in response to this UDF signal 107, and the output 108 (refer to drawing 3 (g)) is inputted into the clock generation circuit 6. The clock generation circuit 6 will be in operating state in response to the signal 108 of "0" outputted from a flip-flop 5, clock signals 109 and 110 are outputted corresponding to the input of the oscillation signal 104 from an oscillator circuit 2, it is sent to the internal circuitry in a semiconductor integrated circuit, and operation of the internal circuitry concerned is started.

[0027] Time T4 If it sets and a stop signal 102 (refer to drawing 3 (h)) is inputted, both the flip-flops 1 and 5 will be set, and the oscillation of an oscillator circuit 2 will stop in response to the signal 103 of "1" outputted from a flip-flop 1's by this. Moreover, the output of the clock signals 109 and 110 corresponding to [while a counter 3 is initialized through a signal 108, operation of the clock generation circuit 6 is stopped, and] the input of the oscillation signal 104 from an oscillator circuit 2 of "1" outputted through a flip-flop 5 is also suspended. For this reason, in this state, the power consumption in a semiconductor integrated circuit serves as the minimum. And again, if a reset signal 101 is set as "1", an oscillator circuit 2 will start an oscillation and, thereby, a counter 4 will be initialized. Moreover, when a reset signal 101 is set as "0", since the amplitude of the clock 104 with which a counter 4 is outputted from an oscillator circuit 2 is sufficient level, increment operation with the imperfect clock 106 is not performed, but decrement operation with the perfect clock 105 is performed immediately. Moreover, by the UDF signal's 107 occurring and outputting it in a counter 4, in this case, the signal 108 outputted from a flip-flop 5 is set to "0", thereby, the clock generation circuit 6 will be in operating state, and sending out of the clock signals 109 and 110 to the internal circuitry of a semiconductor integrated circuit is resumed. That is, since the amplitude level of the oscillation signal 104 outputted from an oscillator circuit 2 has reached predetermined level from the start, operation of a semiconductor integrated circuit can be made to start without oscillation stable time.

[0028] Next, the 2nd example of this invention is explained. Drawing 4 is the block diagram showing the composition of this example. it is shown in drawing 4 -- as -- this example -- flip-flops 1, 5, and 9, an oscillator circuit 2, and counting -- the clock generation circuit 3, a counter 4, the clock generation circuit 8, OR circuit 7, and an inverter 10 are had and constituted -- having -- **** -- counting -- the composition of the clock generation circuit 3 is the same as that of the case of the 1st example shown in drawing 1 , and is formed of the Schmitt trigger inverter 31, the normal type inverter 32, and the EXOR gate The constitutional difference with the 1st example of this example is that the flip-flop 9 and the inverter 10 are newly added.

[0029] in drawing 4 , a flip-flop 1 is an RS flip flop; and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted from the flip-flop 1 concerned is sent to an oscillator circuit 2, and motion control to an

oscillator circuit 2 is performed In this case, while the flip-flop 1 concerned is reset, it is outputted as a signal, and the signal 103 outputted from a flip-flop 1 is outputted as a signal of "1", while ["0"] being set. While the flip-flop 1 is reset in the oscillator circuit 2 in response (a signal 103 is "0"), it will be in an oscillation state and the oscillation signal 104 is outputted, and while the flip-flop 1 is set (a signal 103 is "1"), the signal of a low level is outputted.

[0030] The clock generation circuit 3 is formed of the Schmitt trigger inverter 31, the normal type inverter 32 without a hysteresis characteristic, and the EXOR gate 33 of 2 inputs. counting -- [when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level] In being the clock of amplitude level with the inadequate oscillation signal 104 which the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31, and is outputted from an oscillator circuit 2 The output of the Schmitt trigger inverter 31 and the normal type inverter 32 is outputted as an imperfect clock 106 through the EXOR gate 33.

[0031] a counter 4 -- counting -- it is the up / down counter which carries out decrement operation with the perfect clock 105 outputted from the clock generation circuit 3, and carries out increment operation with the imperfect clock 106, and the UDF signal 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, is inputted into a flip-flop 9 through an inverter 10, and functions as an object for control of an internal reset signal while a signal 108 is outputted and being inputted into a counter 4 through the OR gate 7 in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4. Moreover, in the clock generation circuit 8, the oscillation signal 104 outputted from an oscillator circuit 2 is inputted, the ******** predetermined clock signals 109 and 110 are generated and outputted also to the oscillation signal 104 concerned, and it is sent out to the internal circuitry of a semiconductor integrated circuit. And the newly added flip-flop 9 is an RS flip flop of set priority, and in response to the input of the signal with which the signal 108 outputted from a flip-flop 5 was reversed by the inverter 10, and a reset signal 101, a reset signal 114 is generated and outputted and it is sent out to the internal circuitry of a semiconductor integrated circuit.

[0032] The difference between this example and the 1st above-mentioned example As opposed to operation of the clock generation circuit 6 being controlled by the signal 108 outputted from a flip-flop 5 in the 1st example In the clock generation circuit 8 in this example Corresponding to the input of the oscillation signal 104 outputted from an oscillator circuit 2, it is constituted so that the ** clock signals 109 and 110 may be outputted. In the limitation as which the oscillation signal 104 concerned is inputted, I hear that the ****** clock signals 109 and 110 are outputted from the clock generation circuit 8 to an internal circuitry, and there are.

[0033] Moreover, other differences with the 1st example of this example As a reset signal to the internal circuitry of the semiconductor integrated circuit in the 1st example A reset signal 101 sets to this example to being directly sent out to the internal circuitry concerned as it is. The reset signal 114 to the internal circuitry of a semiconductor integrated circuit is using the signal outputted from a flip-flop 9 as the reset signal 114 concerned through the reversal signal of the output 108 of the flip-flop 5 set in response to the input of a reset signal 101.

[0034] Therefore, in the 1st example mentioned above, after oscillation stable time is secured, clock signals 109 and 110 are outputted, and it contrasts with operation in the internal circuitry of a semiconductor integrated circuit being started. In this example, corresponding to an oscillator circuit 2 operating, it begins and the shell clock signals 109 and 110 are generated, after oscillation stable time is secured, an internal reset signal is canceled, and operation in the internal circuitry of a semiconductor integrated circuit is started. However, about the point that operation of an internal circuitry is started after the oscillation stable passage of time in the case of which [of the above 1st and the 2nd example], it is the same.

[0035] Moreover, when operating with the clock from the outside, without using a resonator, in the

case of this example, in the state where there is no oscillation stable time like the case of the 1st above-mentioned example, it is not necessary to say that an internal reset signal is canceled and operation of the internal circuitry of a semiconductor integrated circuit is started immediately.

[0036] Next, the 3rd example of this invention is explained. Drawing 5 is the block diagram showing the composition of this example. counting in which this example contains flip-flops 1, 5, and 12, an oscillator circuit 2, and the Schmitt trigger inverter 31 and the normal type inverter 32 as shown in drawing 5 -- it has the clock generation circuit 11, a counter 13, the clock generation circuit 6, and the OR gate 7, and is constituted the constitutional difference with the 1st example of this example -- counting -- it is in the content of composition containing the clock generation circuit 11, a flip-flop 12, and a counter 13

[0037] in drawing 5 , like the case of the 1st and 2nd examples, a flip-flop 1 is an RS flip flop of set priority, and is set by the stop signal 102 from a microcomputer -- having -- highness -- it is reset by the active reset signal 101, and the signal 103 outputted from the flip-flop 1 concerned is sent to an oscillator circuit 2, and motion control to an oscillator circuit 2 is performed In this case, the signal 103 outputted from a flip-flop 1 is outputted as a signal of "0", while the flip-flop 1 concerned is reset. Moreover, while being set, in response, it sets in the point of "1" outputted as a signal, and a row at an oscillator circuit 2. While the flip-flop 1 is reset (a signal 103 is "0"), will be in an oscillation state and the oscillation signal 104 will be outputted. It is the same as that of the case of the above-mentioned 1st and the 2nd example that the signal of a low level is outputted while the flip-flop 1 is set (a signal 103 is "1").

[0038] counting -- the amplitude level of the oscillation signal 104 which the clock generation circuit 11 is formed of the Schmitt trigger inverter 31 and the normal type inverter 32 without a hysteresis characteristic, the perfect clock signal 105 is outputted through the Schmitt trigger inverter 31 when the oscillation signal 104 outputted from an oscillator circuit 2 is the clock of sufficient amplitude level, and is outputted from an oscillator circuit 2 is not related how, but the imperfect clock 111 is outputted through the normal inverter 32 a counter 4 -- counting -- counter operation is carried out with the imperfect clock 111 outputted from the clock generation circuit 11, it is in the up / down counter which changes to any of an increment or a decrement they are, and operates in response to the signal outputted from a flip-flop 12, and the UDF signal 107 is generated and outputted corresponding to a predetermined enumerated data Moreover, a flip-flop 5 is an RS flip flop of set priority, and in response to the input of the signal 103 outputted from a flip-flop 1, and the UDF signal 107 outputted from a counter 4, a signal 108 is outputted and it is inputted into the clock generation circuit 6 and the OR gate 7. While operation of the clock generation circuit 6 is controlled through this signal 108, reset of a counter 4 is controlled through the OR gate 7. In the clock generation circuit 6, the oscillation signal 104 outputted from an oscillator circuit 2 is inputted, and the predetermined clock signals 109 and 110 are generated and outputted based on the oscillation signal concerned.

[0039] In the 1st example mentioned above, the decrement of the counter 4 was carried out with the perfect clock 105 which increments a counter 4 with the imperfect clock 106 generated when the amplitude level of the oscillation signal 104 outputted from an oscillator circuit 2 is small, and is generated when amplitude level is sufficient level, and the underflow is detected. counting [as opposed to the direct counter 13 for the imperfect clock 111 which the amplitude level of the oscillation signal 104 is not related how, but is generated in this example as contrasted with this] -- it uses as a clock and the increment in a counter 13 is performed And when it sets after that and the amplitude level of a clock becomes large enough, in the standup of the perfect clock 105 which starts operation, the mode of operation in a counter 13 was changed from the increment to the decrement, and the underflow is detected. In operating by supply of an external clock like the case of the 1st example in the case of this example, in order to go into decrement operation, without performing

increment operation in a counter 13 in order that the perfect clock 105 may operate immediately, oscillation stable time is deleted.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the 1st example of this invention.
[Drawing 2] It is a timing chart of operation at the time of resonator operation in the 1st example.
[Drawing 3] It is a timing chart of operation at the time of external clock supply operation in the 1st example.
[Drawing 4] It is the block diagram showing the 2nd example of this invention.
[Drawing 5] It is the block diagram showing the 3rd example of this invention.
[Drawing 6] It is the block diagram showing the conventional example.
[Drawing 7] They are other conventional ****** block diagrams.
[Description of Notations]
1, 5, 9, 12, 14, 18, 22, 23, 28 Flip-flop
2 19 Oscillator circuit
3 and 11 counting -- clock generation circuit
4, 13, 17, 26 Counter
6 Eight Clock generation circuit
7, 25, 27 OR gate
10, 16, 21, 32 Inverter
15 NOR Gate
20 31 Schmitt trigger inverter
24 VCO
29 Clock Signal Generating Circuit
33 EXOR Gate

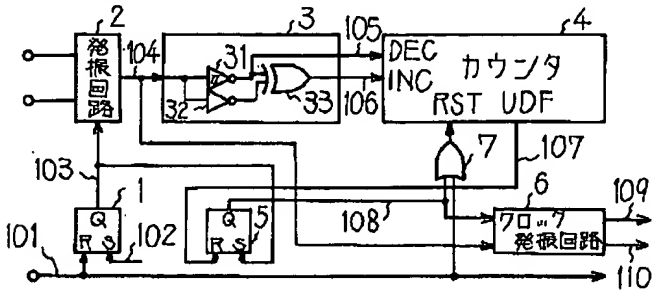
[Translation done.]

* NOTICES *

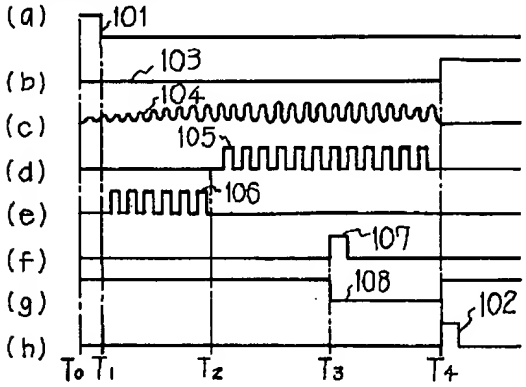
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

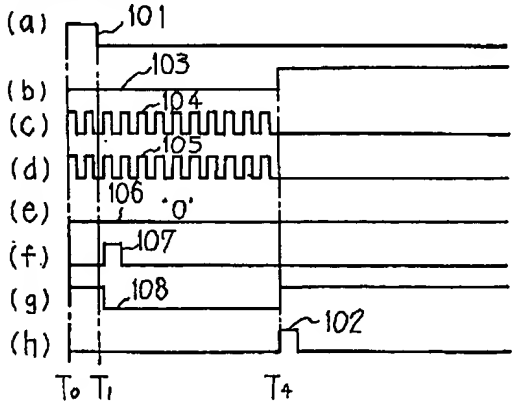
[Drawing 1]



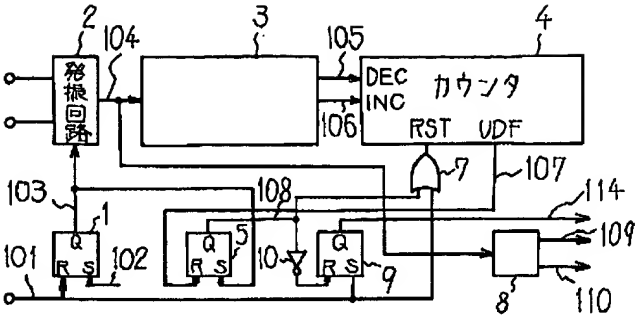
[Drawing 2]



[Drawing 3]

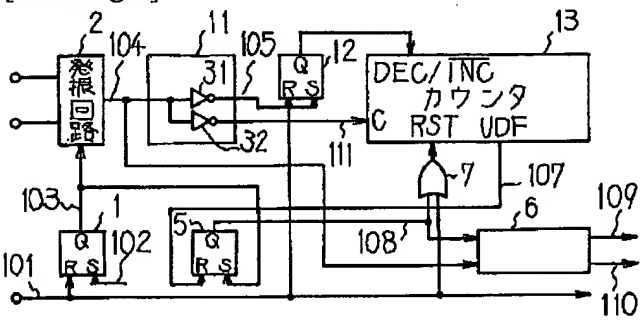


[Drawing 4]



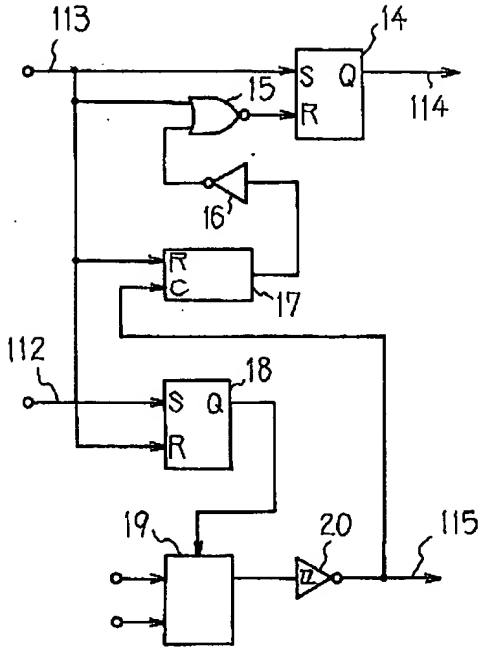
1, 5, 9 … フリップフロップ
3 … 計数クロック生成回路
7 … ORゲート
8 … クロック発生回路
10 … インバータ

[Drawing 5]



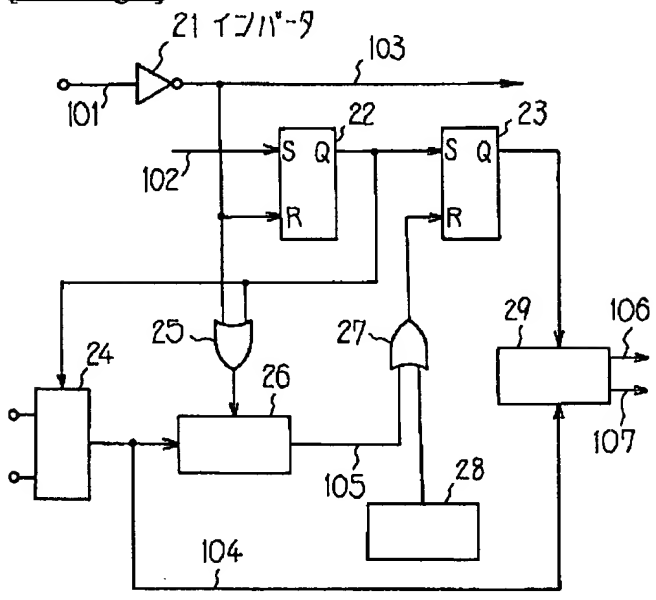
1, 5, 12 … フリップフロップ
7 … ORゲート
11 … 計数クロック生成回路
31 … シュミットトリガインバータ
32 … インバータ

[Drawing 6]



14,18… フリップフロップ
15…NORゲート
16…インバータ
17…カウンタ
19…発振回路
20…シュミットトリガインバータ

[Drawing 7]



22,23,28… フリップフロップ
24…発振器
25,27…ORゲート
26…カウンタ
29…クロック信号発生回路

[Translation done.]

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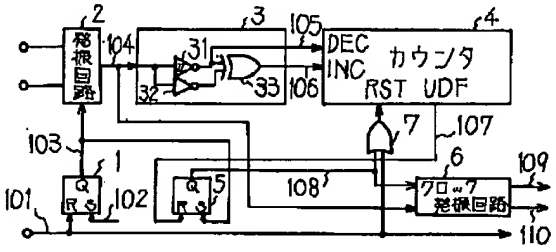
(54)【発明の名称】　スタンバイ制御回路

(57)【要約】

【目的】共振子動作時の立ち上がり安定時間を確保し、外部クロック供給動作時の不要発振安定時間を排除して応答性を改善するスタンバイ制御回路を提供する。

【構成】本発明は、リセット信号１０１とストップ信号１０２を入力して、発振回路２に対する制御信号１０３を出力するフリップフロップ１と、発振回路２の発振出力１０４の振幅レベルに応じて完全クロック１０５および不完全クロック１０６を出力する計数クロック生成回路３と、前記完全クロック１０５および不完全クロック１０６を受けて、デクリメント動作ならびにインクリメント動作を行うとともに、所定の計数値に応じてアンダーフロー信号１０７を出力するカウンタ４と、フリップフロップ１より出力される制御信号１０３とアンダーフロー信号１０７を受けて、クロック発生回路６の動作を制御するフリップフロップ５とを備えて構成される。



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【特許請求の範囲】

【請求項1】　半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、

外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第1の制御信号を出力する第1の制御回路と、

前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、

前記完全クロック信号ならびに不完全クロック信号を入力して、前記完全クロック信号によりデクリメント動作を行い、前記不完全クロック信号によりインクリメント動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、

前記第1の制御回路より出力される第1の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記クロック発生回路の動作を制御するための第2の制御信号を出力する第2の制御回路と、

を少なくとも備えて構成されることを特徴とするスタンバイ制御回路。

【請求項2】　前記第1の制御回路が、外部から供給される制御信号ならびにリセット信号がそれぞれS端子およびR端子に入力され、前記第1の制御信号がQ端子より出力されるフリップフロップにより形成され、前記計数クロック生成回路が、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成されるとともに、前記第2の制御回路が、前記第1の制御信号がS端子に入力され、前記アンダーフロー信号がR端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成される請求項1記載のスタンバイ制御回路。

【請求項3】　半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、

外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第1の制御信号を出力する第1の制御回路と、

前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、

前記完全クロック信号ならびに不完全クロック信号を入力して、前記完全クロック信号によりデクリメント動作を行い、前記不完全クロック信号によりインクリメント動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、

前記第1の制御回路より出力される第1の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記半導体集積回路の内部回路のリセット動作を制御するための第2の制御信号を出力する第2の制御回路と、

前記第2の制御信号の反転信号と、前記外部から供給されるリセット信号とを入力して、前記内部回路に対する内部リセット信号を生成して出力する第3の制御回路と、

を少なくとも備えて構成されることを特徴とするスタンバイ制御回路。

【請求項4】　前記第1の制御回路が、外部から供給される制御信号ならびにリセット信号がそれぞれS端子およびR端子に入力され、前記第1の制御信号がQ端子より出力されるフリップフロップにより形成され、前記計数クロック生成回路が、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成されるとともに、前記第2の制御回路が、前記第1の制御信号がS端子に入力され、前記アンダーフロー信号がR端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成されるとともに、前記第3の制御回路が、前記外部から供給されるリセット信号がS端子に入力され、前記第2の制御信号の反転信号がR端子に入力されて、前記第3の制御信号がQ端子より出力されるフリップフロップにより形成される請求項3記載のスタンバイ制御回路。

【請求項5】　半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、

外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第1の制御信号を出力する第1の制御回路と、

前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、

前記完全クロック信号ならびに前記外部から供給される

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ロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、

前記完全クロック信号ならびに不完全クロック信号を入力して、前記完全クロック信号によりデクリメント動作を行い、前記不完全クロック信号によりインクリメント動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、

前記第1の制御回路より出力される第1の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記半導体集積回路の内部回路のリセット動作を制御するための第2の制御信号を出力する第2の制御回路と、

前記第2の制御信号の反転信号と、前記外部から供給されるリセット信号とを入力して、前記内部回路に対する内部リセット信号を生成して出力する第3の制御回路と、

を少なくとも備えて構成されることを特徴とするスタンバイ制御回路。

【請求項4】　前記第1の制御回路が、外部から供給される制御信号ならびにリセット信号がそれぞれS端子およびR端子に入力され、前記第1の制御信号がQ端子より出力されるフリップフロップにより形成され、前記計数クロック生成回路が、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成されるとともに、前記第2の制御回路が、前記第1の制御信号がS端子に入力され、前記アンダーフロー信号がR端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成されるとともに、前記第3の制御回路が、前記外部から供給されるリセット信号がS端子に入力され、前記第2の制御信号の反転信号がR端子に入力されて、前記第3の制御信号がQ端子より出力されるフリップフロップにより形成される請求項3記載のスタンバイ制御回路。

【請求項5】　半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、

外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第1の制御信号を出力する第1の制御回路と、

前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、

前記完全クロック信号ならびに前記外部から供給される

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リセット信号により制御され、第2の制御信号を出力する第2の制御回路と、
前記第2の制御信号により制御されてインクリメントまたはデクリメントを切替えて動作し、前記不完全クロック信号を入力して計数動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、
前記第1の制御回路より出力される第1の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記クロック発生回路の動作を制御するための第3の制御信号を出力する第3の制御回路と、
を少なくとも備えて構成されることを特徴とするスタンバイ制御回路。

【請求項6】　前記第1の制御回路が、外部から供給される制御信号ならびにリセット信号がそれぞれS端子およびR端子に入力され、前記第1の制御信号がQ端子より出力されるフリップフロップにより形成され、前記第2の制御回路が、前記外部から供給されるリセット信号がR端子に入力され、前記完全クロック信号がS端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成されて、前記計数クロック生成回路が、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して前記不完全クロックを出力するインバータとにより形成されるとともに、前記第3の制御回路が、前記第1の制御信号がS端子に入力され、前記アンダーフロー信号がR端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成される請求項5記載のスタンバイ制御回路。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明はスタンバイ制御回路に関し、特にクロック信号発生回路を内蔵して、半導体集積回路における内外クロック信号を制御するスタンバイ制御回路に関する。

【0002】

【従来の技術】最近における半導体集積回路、特に当該半導体集積回路により形成されるマイクロコンピュータにおいては、低消費電力化を求める要求が極めて強く、これに対応するためにCMOS技術の採用が進められている。また、このCMOS技術化に加えて、更にマイクロコンピュータのスタンバイ時においては、クロックを発生するための発振回路より出力される原発振クロックを停止し、これにより当該マイクロコンピュータに含まれる半導体集積回路の回路動作を禁止することによって、消費電力の極小化を図った半導体集積回路が開発されている。

【0003】これらのマイクロコンピュータにおけるスタンバイ状態の設定は、一般的には、ユーザープログラムにより、対応する命令を実行することによって行われており、当該命令により前記発振回路による原発振クロックの停止処理が実行される。またこれとは逆に、マイクロコンピュータのスタンバイ状態を解除する場合に、リセット端子番号などにより原発振の開始処理が行われ、所定のアドレスよりユーザープログラムの実行が開始される。その際、発振回路の立ち上がり時においてはクロックが安定した状態にないため、当該発振回路による発振が安定するまでの所定時間経過後において内部クロックとしての供給を行うか、または、発振が安定するまでの前記所定時間に対応するカウント数を設定されたカウンタを、クロックの発振出力によりインクリメント動作させて、前記設定カウント数に到達した時点において発生するオーバーフロー信号により内部リセットを解除することによって、クロック発振回路の発振安定時間を確保して、安定したクロックによりプログラムの実行が開始されるようにシステムが構成されている。

【0004】図6は、従来のスタンバイ制御回路の一例を示す図である。スタンバイ時においては、マイクロコンピュータより送られてくる停止命令112によりフリッププロップ18がセットされ、フリッププロップ18の出力を受けて発振回路19のクロック発振は停止される。スタンバイ解除は、外部からのアクティブなリセット信号113によりフリップフロップ18がリセットされることにより行われる。セットされたフリップフロップ18の出力を受けて、発振回路12におけるクロック発振が再開される。そして同時に、フリップフロップ14より出力される内部リセット信号114もアクティブになるが、フリップフロップ18に対するリセット解除は、発振回路19の発振出力がシュミットトリガインバータ20を介して出力される内部クロック信号の、カウンタ17におけるカウント数が所定値に達した後において、フリップフロップ14がリセットされて行われる。従って、プログラム実行の再開は、カウンタ17における所定のカウント時間経過後において、始めて発振判定安定時間が確保されている。

【0005】このような従来のスタンバイ回路においては、共振子を用いずに、外部クロックの供給を受けてマイクロコンピュータを動作させるシステムの場合においても、前述の発振安定時間の経過後でないと再動作させることができないため、応答性が悪いという問題点が介在している。この問題点に対処するために、他の従来例として、特開平5－277809号公報（特願平3－39650号公報）においてクロック信号制御回路が提案されている。本提案によるクロック信号制御回路は、共振子を用いる発振回路と、当該発振回路の出力信号にもとづいてクロック信号を発生するクロック信号発生回路とを備えるクロック信号制御回路において、外部からの制御信号とリセット信号により制御され、前記発振回路

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の動作を制御する第１の制御回路と、前記第１の制御回路により初期化され、前記発振回路の出力信号を計数して、予め定めた計数値に到達した時に計数信号を出力する計数回路と、前記計数信号を制御する第２の制御回路と、前記第１および第２の制御回路により前記クロック発生回路の動作を制御する第３の制御回路とを備えることを特徴としている。

【０００６】図７は、当該提案によるクロック信号制御回路の実施例を示す図であり、マイクロコンピュータのクロック信号制御回路として適用された例である。図７に示されるように、本従来例は、インバータ２１と、第１の制御回路として機能するフリップフロップ２２と、第２の制御回路として機能するフリップフロップ２８と、第３の制御回路として機能するフリップフロップ２３と、共振子を用いた発振器２４と、ＯＲゲート２５および２７と、カウンタ２６と、クロック発生回路２９とを備えて構成されており、フリップフロップ２３のリセットは、カウンタ２６の出力と、予め外部クロックによる動作か共振子を用いる発振器による動作かを示すフリップフロック２８の出力とにより設定されている。

【０００７】フリップフロップ２２はＲＳフリップフロップであり、マイクロコンピュータのストップ命令１０２によりセットされ、ローレベルのリセット信号１０１がインバータ２１により反転されて出力されるアクティブのリセット信号１０３によりリセットされて、その出力により発振器２４の動作を制御する。カウンタ２６は、発振器２４の発振出力１０４を計数し、一定時間の経過後において所定の計数値に達するとオーバーフロー信号１０５を出力する。フリップフロップ２８は、電源投入時には論理“０”に初期化され、特定命令の実行によりセットされるパワーオンフリップフロップである。また、フリップフロップ２３は、セット優先のＲＳフリップフロップであり、フリップフロップ２２の出力と、ＯＲゲート２７の出力を受けて、クロック発生回路２９の動作を制御する。そして、クロック発生回路２９からは、発振器２４の発振出力１０４およびフリップフロップ２３からの制御信号を受けて、クロック信号１０６および１０７が出力される。

【０００８】フリップフロップ２８の動作は、外部信号またはマイクロコンピュータの命令等による信号によって制御されるが、本実施例においては、フリップフロップ２８の出力信号は、予め外部クロック動作時においては“１”に設定され、共振子を用いる発振器による動作時においては“０”に設定される。スタンバイ解除動作において、共振子動作の場合にはフリップフロップ２８の出力信号は“０”に設定され、図６の従来例の場合と同様に、カウンタ２６の計数値が所定値に達するとフリップフロップ２３がリセットされ、発振安定時間が確保された状態になってからクロックが動作してプログラムが実行される。また他方、外部クロック動作時においては、フリップフロップ２８の出力は“１”に設定され、これにより、スタンバイ解除時においては、カウンタ２６のカウント値に関わらず外部からのリセット信号１０１が解除されると同時に、フリップフロップ２３もリセットされるために、クロックが動作しプログラムの実行が再開される。従って、共振子を用いた発振器２４の立ち上がり時の安定時間を確保することができるとともに、外部からのクロックを受ける場合においても、発振安定のための余分の待ち時間を削除することができるものとしており、不要な発振安定時間を待つことがなく応答性がよいとしている。

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【０００９】

【発明が解決しようとする課題】上述した従来のスタンバイ制御回路においては、内蔵される発振回路として共振子を用いずに、外部クロックの供給を受けてマイクロコンピュータを動作させるシステムの場合においても、立ち上がり時点から安定したクロックが得られるにもかかわらず、発振安定時間を確保するためのカウンタが動作するまでに時間を要し、当該マイクロコンピュータの再動作時の応答性が低下するという欠点がある。

【００１０】また、上記の欠点を解決する方法として、特開平４－２７７８０９号公報（特願平３－３９６５０号公報）が提案されているが、この提案においては、命令の追加もしくは端子の追加等が必要となり、回路規模の増大およびコストの増大を招くという欠点がある。

【００１１】また、共振子動作であるか、または外部クロック動作であるかを予め設定することが必要となるために、システム変更等に対しては、対応するプログラムをも変更せざるを得なくなるという柔軟性に欠ける欠点がある。

【００１２】

【課題を解決するための手段】第１の発明のスタンバイ制御回路は、半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第１の制御信号を出力する第１の制御回路と、前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、前記完全クロック信号ならびに不完全クロック信号を入力して、前記完全クロック信号によりデクリメント動作を行い、前記不完全クロック信号によりインクリメント動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、前記第１の制御回路より出力される第１の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御する

とともに、前記クロック発生回路の動作を制御するための第２の制御信号を出力する第２の制御回路と、を少なくとも備えて構成される。

【００１３】なお、第１の発明における前記第１の制御回路としては、外部から供給される制御信号ならびにリセット信号がそれぞれＳ端子およびＲ端子に入力され、前記第１の制御信号がＱ端子より出力されるフリップフロップにより形成し、前記計数クロック生成回路は、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成するとともに、前記第２の制御回路は、前記第１の制御信号がＳ端子に入力され、前記アンダーフロー信号がＲ端子に入力されて、前記第２の制御信号がＱ端子より出力されるフリップフロップにより形成してもよい。

【００１４】また、第２の発明のスタンバイ制御回路は、半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第１の制御信号を出力する第１の制御回路と、前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、前記完全クロック信号ならびに不完全クロック信号を入力して、前記完全クロック信号によりデクリメント動作を行い、前記不完全クロック信号によりインクリメント動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、前記第１の制御回路より出力される第１の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記半導体集積回路の内部回路のリセット動作を制御するための第２の制御信号を出力する第２の制御回路と、前記第２の制御信号の反転信号と、前記外部から供給されるリセット信号とを入力して、前記内部回路に対する内部リセット信号を生成して出力する第３の制御回路と、を少なくとも備えて構成される。

【００１５】なお、第２の発明における前記第１の制御回路は、外部から供給される制御信号ならびにリセット信号がそれぞれＳ端子およびＲ端子に入力され、前記第１の制御信号がＱ端子より出力されるフリップフロップにより形成し、前記計数クロック生成回路は、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成して、前記第２の制御回路は、前記第１の制御信号がＳ端子に入力され、前記アンダーフロー信号がＲ端子に入力されて、前記第２の制御信号がＱ端子より出力されるフリップフロップにより形成するとともに、前記第３の制御回路は、前記外部から供給されるリセット信号がＳ端子に入力され、前記第２の制御信号の反転信号がＲ端子に入力されて、前記第３の制御信号がＱ端子より出力されるフリップフロップにより形成してもよい。

【００１６】更に、第３の発明のスタンバイ制御回路は、半導体集積回路内の内部回路に供給されるクロック信号を生成するための共振子を用いる発振回路と、当該発振回路の発振出力信号にもとづいて前記クロック信号を発生するクロック発生回路とを含むスタンバイ制御回路において、外部から供給される制御信号ならびにリセット信号により制御され、前記発振回路の動作を制御するための第１の制御信号を出力する第１の制御回路と、前記発振回路の発振出力信号の振幅レベルを検出して、当該振幅レベルに対応する完全クロック信号と不完全クロック信号とを、それぞれ分離して生成して出力する計数クロック生成回路と、前記完全クロック信号ならびに前記外部から供給されるリセット信号により制御され、第２の制御信号を出力する第２の制御回路と、前記第２の制御信号により制御されてインクリメントまたはデクリメントを切替えて動作し、前記不完全クロック信号を入力して計数動作を行うとともに、所定の計数値に対応してアンダーフロー信号を出力する計数回路と、前記第１の制御回路より出力される第１の制御信号と、前記計数回路より出力されるアンダーフロー信号とを入力して、前記計数回路の初期化を制御するとともに、前記クロック発生回路の動作を制御するための第３の制御信号を出力する第３の制御回路と、を少なくとも備えて構成される。

【００１７】なお、第３の発明における前記第１の制御回路は、外部から供給される制御信号ならびにリセット信号がそれぞれＳ端子およびＲ端子に入力され、前記第１の制御信号がＱ端子より出力されるフリップフロップにより形成し、前記第２の制御回路は、前記外部から供給されるリセット信号がＲ端子に入力され、前記完全クロック信号がＳ端子に入力されて、前記第２の制御信号がＱ端子より出力されるフリップフロップにより形成して、前記計数クロック生成回路は、前記発振回路の発振出力信号を入力して前記完全クロック信号を出力するシュミットトリガインバータと、前記発振回路の発振出力信号を入力して反転して出力するインバータと、これらのシュミットトリガインバータおよびインバータの出力を入力して前記不完全クロックを出力するＥＸＯＲゲートとにより形成して、前記第３の制御回路は、前記第１の制御信号がＳ端子に入力され、前記アンダー

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フロー信号がR端子に入力されて、前記第2の制御信号がQ端子より出力されるフリップフロップにより形成してもよい。

【0018】

【実施例】次に、本発明について図面を参照して説明する。

【0019】図1は本発明の第1の実施例を示すブロック図である。図1に示されるように、本実施例は、フリップフロップ1および5と、発振回路2と、シュミットトリガインバータ31、インバータ32およびEXORゲート33を含む計数クロック生成回路3と、カウンタ4と、クロック発生回路6と、OR回路7とを備えて構成される。

【0020】図1において、フリップフロップ1はRSフリップフロップであり、マイクロコンピュータからのストップ信号102によりセットされ、ハイアクティブのリセット信号101によりリセットされて、出力される信号103は発振回路2に送られて、当該発振回路に対する動作制御が行われる。なおフリップフロップ1がセットされている間においては、その出力として、ロウレベルの信号103が出力される。当該フリップフロップ2より出力される“0”の信号103を受けて発振回路2が発振状態となり、当該発振回路2からは発振信号104が出力されて、計数クロック生成回路3およびクロック発生回路合6に入力される。計数クロック生成回路3は、シュミットトリガインバータ31、ヒステリシス特性を持たないノーマルタイプのインバータ32および2入力のEXORゲート33により形成されており、発振回路2より出力される発振信号104が十分な振幅レベルのクロックの場合においては、シュミットトリガインバータ31を介して完全クロック信号105が出力され、また発振回路2より出力される発振信号104が不十分な振幅レベルのクロックの場合には、シュミットトリガインバータ31とノーマルインバータ32の出力のEXORゲート33を介して不完全クロック106が出力される。

【0021】カウンタ4は、計数クロック生成回路3より出力される完全クロック105によりデクリメント動作し、また不完全クロック106によりインクリメント動作するアップ／ダウンカウンタであり、所定の計数値に対応してアンダーフロー信号（以下、UDF信号と云う）107が生成されて出力される。また、フリップフロップ5はセット優先のRSフリップフロップであり、フリップフロップ1より出力される信号103と、カウンタ4より出力されるUDF信号107の入力を受けて、信号108が出力されてクロック発生回路6およびORゲート7に入力される。この信号108を介してクロック発生回路6の動作が制御されるとともに、カウンタ4のリセットが制御される。クロック発生回路6においては、発振回路2より出力されるクロック信号104

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が入力され、当該クロック信号にもどづいて所定のクロック信号109および110が生成されて出力される。

【0022】図2（a）、（b）、（c）、（d）、（e）、（f）、（g）および（h）は、本実施例の共振子を用いた場合における各部の信号を示すタイミング図であり、また、図3（a）、（b）、（c）、（d）、（e）、（f）、（g）および（h）は、本実施例の外部からクロックパルスの供給を受ける場合における各部の信号を示すタイミング図である。

【0023】次に、最初に、図1および図2の参照して、本実施例の共振子を用いた場合における動作について説明する。まず、時刻T_0において電源が投入され、リセット信号101（図2（a）参照）が“1”になると、フリップフロップ1およびカウンタ4と、当該半導体集積回路内の内部回路等が初期化される。また、フリップフロップ5より出力される信号108（図2（g）参照）は“0”または“1”の何れであっても、電源投入時のリセット信号101が、通常発振の安定に十分な時間の間において“1”となっているために問題がないが、ここでは便宜上“1”であるものとする。従って、発振回路2が発振状態にあっても、クロック発生回路6に入力される信号108が“1”であるためにクロック発生回路6は停止状態にある。また、フリップフロップ1から出力される信号103（図2（b）参照）が“0”であるために、発振回路2が発振を開始し、当該発振回路2より出力される発振信号104（図2（c）参照）の振幅レベルは、次第に大きいレベルになってゆく。次いで、時刻T_1においてはリセット信号101が“0”になるが、フリップフロップ5より出力される信号108が“1”であるために、クロック信号109および110はクロック発生回路6より出力されることがない。カウンタ4においては、リセットが解除されてカウンタが開始されるが、発振回路2より出力される発振信号104の振幅が小さいために、シュミットトリガインバータ31はこれには感応せず、ノーマルインバータ32からのみクロック信号が伝達され、完全クロック信号105（図2（d）参照）は停止状態となって、不完全クロック106（図2（e）参照）のみが動作するために、これを受けてカウンタ4においてはインクリメント動作が行われる。

【0024】時刻T_2においては、クロック信号104の振幅レベルが成長して、シュミットトリガインバータ31が感応する所定レベルに達すると、不完全クロック105は停止し、完全クロック106の動作が開始される。従って、カウンタ4においては、その動作がインクリメント動作からデクリメント動作に移行する。そして、時刻T_3においては、カウンタ4がアンダーフローしてUDF信号107が出力されると、これを受けて、フリップフロップ5がリセットされ、フリップフロップ5より出力される“1”の信号108を介してクロック

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発生回路6が動作状態となり、発振信号104を受けて、当該クロック発生回路6からはクロック信号109および110が出力され、半導体集積回路内の内部回路に送出される。そして時刻T_4において、外部からのストップ信号102（図2（h）参照）が入力されると、これを受けてフリップフロップ1および5は共にセットされ、フリップフロップ1より出力される“1”の信号103を受けて発振回路2の発振は停止され、カウンタ4が初期化されるとともに、フリップフロップ5より出力される“1”の信号108を受けてクロック発生回路6からのクロック信号109および110の出力も停止される。このために、半導体集積回路における消費電力は極小の状態となる。

【0025】そして、再度リセット信号101を“1”とすることにより、フリッフフロップ1の出力103を介して発振回路2の発振が開始され、またORゲート7を介してカウンタ4が初期化される。リセット信号101を“0”にすることにより、カウンタ4は、前述のように、発振信号104の振幅レベルが不十分な期間においては、計数クロック生成回路3より出力される不完全クロック105によりインクリメント動作が行われ、また所定の振幅レベルに達した後においては完全クロック106によりデクリメント動作が行われる。また、カウンタ4おいてUDF信号107が発生されて出力されることにより、フリップフロップ5の出力108を介して、クロック発生回路6よりはクロック信号109および110の出力が再開される。即ち、発振回路3より出力される発振信号104の振幅レベルが、所定レベルに達するまでの時間に応じた発振安定時間を確保することが可能となる。

【0026】次に、図1および図3を参照して、外部からクロックパルスの供給を受ける場合における、本実施例の動作について説明する。なお、ここにおいては、前述の共振子を用いた場合における本実施例の動作と重複する点については説明を省略し、前述の図2（a）、（b）、（c）、（d）、（e）、（f）、（g）および（h）のタイミング図に示される動作とは異なる点について説明するものとする。図1における発振回路2より出力される発振信号104（図3（c）参照）は、外部からのクロックの供給を受ける状態にあるため、時刻T_0においては、フリップフロップ1に入力されるリセット信号101（図3（a）参照）がアクティブになると、当該フリップフロップ1より出力される“0”の信号103（図3（b）参照）を受けて直ちに十分な振幅レベルで発振を開始する。従って、シュミットトリガインバータ31およびノーマルインバータ32からも同様にクロック信号が伝達されて、完全クロック105（図3（d）参照）が動作状態となって出力され、不完全クロック106（図3（e）参照）は停止状態となる。これに対応して、時刻T_1においてカウンタ4がリセット

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を解除されるとデクリメント動作が行われ、カウンタ4よりは、1クロック後にUDF信号107（図3（f）参照）が出力されてフリップフロップ5に入力される。フリップフロップ5においては、このUDF信号107をリセット端子に受けてリセットされ、その出力108（図3（g）参照）はクロック発生回路6に入力される。クロック発生回路6は、フリップフロップ5より出力される“0”の信号108を受けて動作状態となり、発振回路2からの発振信号104の入力に対応してクロック信号109および110が出力され、半導体集積回路内の内部回路に送られて、当該内部回路の動作が開始される。

【0027】時刻T_4においてストップ信号102（図3（h）参照）が入力されると、フリップフロップ1および5が共にセットされ、これによりフリップフロップ1のより出力される“1”の信号103を受けて発振回路2の発振は停止される。また、フリップフロップ5を介して出力される“1”の信号108を介してカウンタ3が初期化されるとともにクロック発生回路6の動作が停止され、発振回路2からの発振信号104の入力に対応するクロック信号109および110の出力も停止される。このため、この状態においては、半導体集積回路における消費電力は極小となる。そして、再度、リセット信号101が“1”に設定されると、これにより発振回路2は発振を開始しカウンタ4は初期化される。また、リセット信号101が“0”に設定される場合には、カウンタ4は、発振回路2より出力されるクロック104の振幅が十分なレベルであるために、不完全クロック106によるインクリメント動作は行われず、直ちに完全クロック105によるデクリメント動作が行われる。また、この場合には、カウンタ4においてUDF信号107が発生して出力されることにより、フリップフロップ5より出力される信号108が“0”となり、これにより、クロック発生回路6が動作状態となって、半導体集積回路の内部回路に対するクロック信号109および110の送出が再開される。即ち、発振回路2より出力される発振信号104の振幅レベルが始めから所定レベルに達しているために、発振安定時間なしに半導体集積回路の動作を開始させることができる。

【0028】次に、本発明の第2の実施例について説明する。図4は、本実施例の構成を示すブロック図である。図4に示されるように、本実施例は、フリップフロップ1、5および9と、発振回路2と、計数クロック生成回路3と、カウンタ4と、クロック発生回路8と、OR回路7と、インバータ10とを備えて構成されており、計数クロック生成回路3の構成は、図1に示される第1の実施例の場合と同様であり、シュミットトリガインバータ31、ノーマルタイプのインバータ32およびEXORゲート33により形成されている。本実施例の第1の実施例との構成上の相違点は、新たにフリップフ

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ロップ９とインバータ１０が付加されていることである。

【００２９】図４において、フリップフロップ１はＲＳフリップフロップであり、マイクロコンピュータからのストップ信号１０２によりセットされ、ハイアクティブのリセット信号１０１によりリセットされて、当該フリップフロップ１より出力される信号１０３は発振回路２に送られて、発振回路２に対する動作制御が行われる。この場合に、フリップフロップ１より出力される信号１０３は、当該フリップフロップ１がリセットされている間においては“０”の信号として出力され、またセットされている間においては“１”の信号として出力される。これを受けて発振回路２においては、フリップフロップ１がリセット（信号１０３が“０”）されている間においては発振状態となって発振信号１０４が出力され、フリップフロップ１がセット（信号１０３が“１”）されている間においてはロウレベルの信号が出力される。

【００３０】計数クロック生成回路３は、シュミットトリガインバータ３１、ヒステリシス特性を持たないノーマルタイプのインバータ３２および２入力のＥＸＯＲゲート３３により形成されており、発振回路２より出力される発振信号１０４が十分な振幅レベルのクロックの場合においては、シュミットトリガインバータ３１を介して完全クロック信号１０５が出力され、また発振回路２より出力される発振信号１０４が不十分な振幅レベルのクロックの場合には、シュミットトリガインバータ３１とノーマルタイプのインバータ３２との出力が、ＥＸＯＲゲート３３を介して不完全クロック１０６として出力される。

【００３１】カウンタ４は、計数クロック生成回路３より出力される完全クロック１０５によりデクリメント動作し、また不完全クロック１０６によりインクリメント動作するアップ／ダウンカウンタであり、所定の計数値に対応してＵＤＦ信号１０７が生成されて出力される。また、フリップフロップ５はセット優先のＲＳフリップフロップであり、フリップフロップ１より出力される信号１０３と、カウンタ４より出力されるＵＤＦ信号１０７の入力を受けて、信号１０８が出力されてＯＲゲート７を介してカウンタ４に入力されるとともに、インバータ１０を介してフリップフロップ９に入力され、内部リセット信号の制御用として機能する。また、クロック発生回路８においては、発振回路２より出力される発振信号１０４が入力されて、当該発振信号１０４にもとづいて所定のクロック信号１０９および１１０が生成されて出力され、半導体集積回路の内部回路に送出される。そして、新たに付加されたフリップフロップ９は、セット優先のＲＳフリップフロップであり、フリップフロップ５より出力される信号１０８がインバータ１０により反転された信号と、リセット信号１０１との入力を受け

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て、リセット信号１１４が生成されて出力され、半導体集積回路の内部回路に送出される。

【００３２】本実施例と前述の第１の実施例との相違点は、第１の実施例においては、クロック発生回路６の動作が、フリップフロップ５より出力される信号１０８により制御されているのに対して、本実施例におけるクロック発生回路８においては、発振回路２より出力される発振信号１０４の入力に対応して、即クロック信号１０９および１１０が出力されるように構成されており、当該発振信号１０４が入力されている限りにおいては、必らずクロック信号１０９および１１０が、クロック発生回路８より内部回路に対して出力されるということである。

【００３３】また、本実施例の第１の実施例との他の相違点は、第１の実施例における半導体集積回路の内部回路に対するリセット信号として、リセット信号１０１が、そのまま直接当該内部回路に送出されているのに対して、本実施例においては、半導体集積回路の内部回路に対するリセット信号１１４は、リセット信号１０１の入力を受けてセットされるフリップフロップ５の出力１０８の反転信号を介して、フリップフロップ９より出力される信号を、当該リセット信号１１４として用いていることである。

【００３４】従って、前述した第１の実施例においては、発振安定時間が確保された後にクロック信号１０９および１１０が出力され、半導体集積回路の内部回路における動作が開始されるのに対比して、本実施例においては、発振回路２が動作するのに対応して、始めからクロック信号１０９および１１０が発生されており、発振安定時間が確保された後に内部リセット信号が解除されて、半導体集積回路の内部回路における動作が開始される。但し、上記の第１および第２の実施例の何れの場合においても、発振安定時間の経過後において、内部回路の動作が開始される点については同様である。

【００３５】また、共振子を用いずに外部からのクロックにより動作する場合においても、前述の第１の実施例の場合と同様に発振安定時間がない状態において、本実施例の場合には、内部リセット信号が解除されて、直ちに半導体集積回路の内部回路の動作が開始されることは云うまでもない。

【００３６】次に、本発明の第３の実施例について説明する。図５は、本実施例の構成を示すブロック図である。図５に示されるように、本実施例は、フリップフロップ１、５および１２と、発振回路２と、シュミットトリガインバータ３１およびノーマルタイプのインバータ３２を含む計数クロック生成回路１１と、カウンタ１３と、クロック発生回路６と、ＯＲゲート７とを備えて構成されている。本実施例の第１の実施例との構成上の相違点は、計数クロック生成回路１１、フリップフロップ１２およびカウンタ１３を含む構成内容にある。

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【００３７】図５において、フリップフロップ１は、第１および第２の実施例の場合と同様に、セット優先のＲＳフリップフロップであり、マイクロコンピュータからのストップ信号１０２によりセットされ、ハイアクティブのリセット信号１０１によりリセットされて、当該フリップフロップ１より出力される信号１０３は発振回路２に送られて、発振回路２に対する動作制御が行われる。この場合に、フリップフロップ１より出力される信号１０３が、当該フリップフロップ１がリセットされている間においては“０”の信号として出力され、またセットされている間においては“１”の信号として出力される点、ならびに、これを受けて発振回路２において、フリップフロップ１がリセット（信号１０３が“０”）されている間においては発振状態となって発振信号１０４が出力され、フリップフロップ１がセット（信号１０３が“１”）されている間においてはロウレベルの信号が出力されることは、前述の第１および第２の実施例の場合と同様である。

【００３８】計数クロック生成回路１１は、シュミットトリガインバータ３１と、ヒステリシス特性を持たないノーマルタイプのインバータ３２により形成されており、発振回路２より出力される発振信号１０４が十分な振幅レベルのクロックの場合においては、シュミットトリガインバータ３１を介して完全クロック信号１０５が出力され、また発振回路２より出力される発振信号１０４の振幅レベルの如何に関せず、ノーマルインバータ３２を介しては不完全クロック１１１が出力される。カウンタ４は、計数クロック生成回路１１より出力される不完全クロック１１１によりカウンタ動作し、フリップフロップ１２より出力される信号を受けてインクリメントまたはデクリメントの何れかに切替えて動作するアップ／ダウンカウンタでであり、所定の計数値に対応してＵＤＦ信号１０７が生成されて出力される。また、フリップフロップ５はセット優先のＲＳフリップフロップであり、フリップフロップ１より出力される信号１０３と、カウンタ４より出力されるＵＤＦ信号１０７の入力を受けて、信号１０８が出力されてクロック発生回路６およびＯＲゲート７に入力される。この信号１０８を介してクロック発生回路６の動作が制御されるとともに、ＯＲゲート７を介してカウンタ４のリセットが制御される。クロック発生回路６においては、発振回路２より出力される発振信号１０４が入力され、当該発振信号にもとづいて所定のクロック信号１０９および１１０が生成されて出力される。

【００３９】前述した第１の実施例においては、発振回路２より出力される発振信号１０４の振幅レベルが小さい場合に発生する不完全クロック１０６によりカウンタ４をインクリメントし、また振幅レベルが十分なレベルの場合に発生する完全クロック１０５によりカウンタ４をデクリメントしてアンダーフローを検出している。これに対比して、本実施例においては、発振信号１０４の振幅レベルの如何に関せず発生する不完全クロック１１１を、直接カウンタ１３に対する計数クロックとして用いて、カウンタ１３におけるインクリメントが行われている。そして、その後において、クロックの振幅レベルが十分に大きくなった時点において、動作を開始する完全クロック１０５の立ち上がりにおいて、カウンタ１３における動作モードをインクリメントからデクリメントに切替えて、アンダーフローを検出している。本実施例の場合においても、第１の実施例の場合と同様に、外部クロックの供給により動作する場合には、完全クロック１０５が直ちに動作するために、カウンタ１３においては、インクリメント動作を行うことなくデクリメント動作に入るため、発振安定時間が削除される。

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【００４０】

【発明の効果】以上説明したように、本発明は、共振子を用いた場合における発振回路の立ち上がり時の安定時間が確保されるとともに、外部からのクロック供給により動作する場合には、発振安定のための無駄な待ち時間を排除して応答性を向上させることができるという効果がある。

【００４１】また、スタンバイ回路自身が共振子を用いた動作であるか、または外部クロック供給による動作であるかを認識することにより、ユーザーとしては、クロック供給の方法を意識することなくプログラムならびにシステムを構築することができるという効果がある。

【００４２】更に、本発明においては、立ち上がりが速い程自動的に安定時間が短縮され、また立ち上がりが遅い程自動的に安定時間が長く設定されるために、共振子の温度等による周囲条件により変化する立ち上がり時間に適応した安定時間が確保されるという効果がある。

【図面の簡単な説明】

【図１】本発明の第１の実施例を示すブロック図である。

【図２】第１の実施例における共振子動作時の動作タイミング図である。

【図３】第１の実施例における外部クロック供給動作時の動作タイミング図である。

【図４】本発明の第２の実施例を示すブロック図である。

【図５】本発明の第３の実施例を示すブロック図である。

【図６】従来例を示すブロック図である。

【図７】他の従来例示すブロック図である。

【符号の説明】

１、５、９、１２、１４、１８、２２、２３、２８　フリップフロップ

２、１９　発振回路

３、１１　計数クロック生成回路

４、１３、１７、２６　カウンタ

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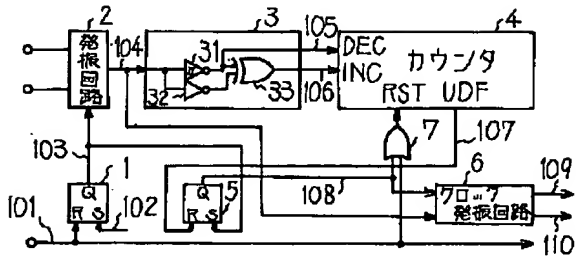
6、8　クロック発生回路
7、25、27　ORゲート
10、16、21、32　インバータ
15　NORゲート

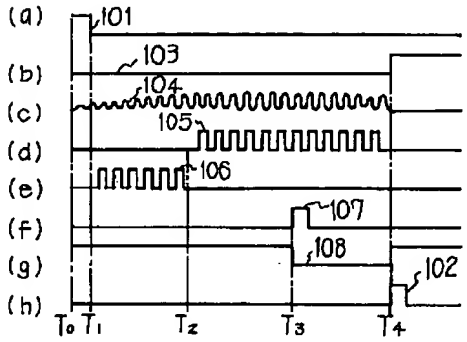
18

20、31　シュミットトリガインバータ
24　発振器
29　クロック信号発生回路
33　EXORゲート

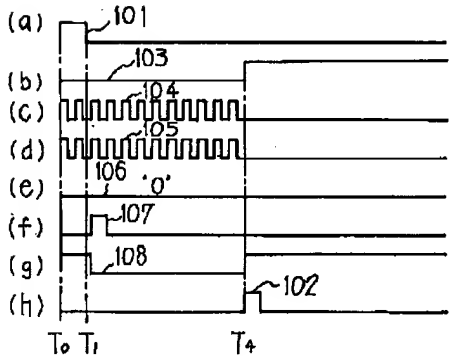
【図1】



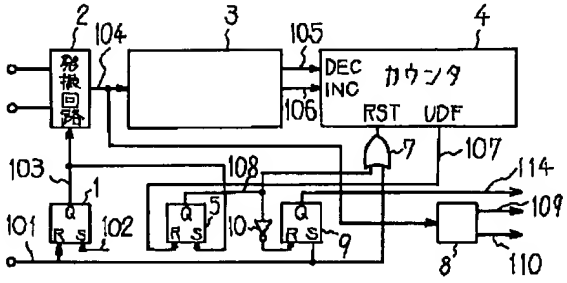
【図2】



【図3】

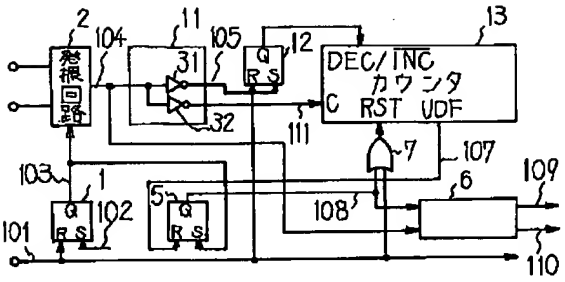


【図4】



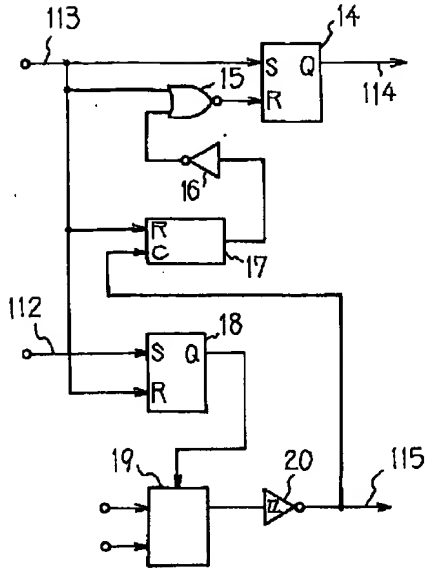
1, 5, 9 … フリップフロップ
3 … 計数クロック生成回路
7 … ORゲート
8 … クロック発生回路
10 … インバータ

【図5】



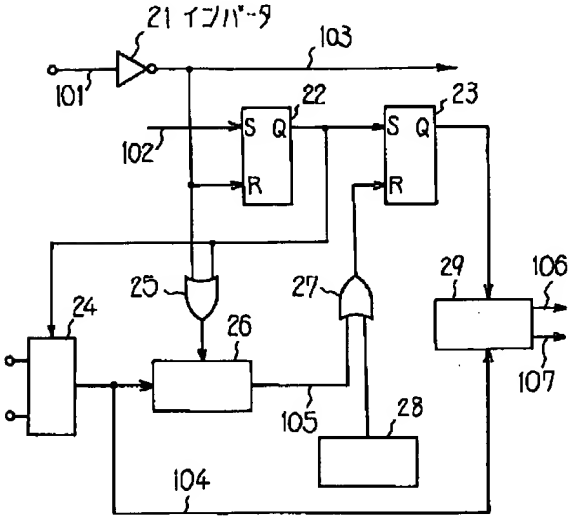
1,5,12… フリップフロップ
7… ORゲート
11… 計数クロック生成回路
31… シュミットトリガインバータ
32… インバータ

【図6】



14,18… フリップフロップ
15…NORゲート
16… インバータ
17… カウンタ
19… 発振回路
20… シュミットトリガインバータ

【図7】



22,23,28… フリップフロップ
24… 発振器
25,27… ORゲート
26… カウンタ
29… クロック信号発生回路